(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 548 995 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92122070.3**

(51) Int. Cl.5: **H04L 12/56**

(22) Date of filing: **28.12.92**

(30) Priority: **26.12.91 JP 344631/91**
27.02.92 JP 40793/92

(43) Date of publication of application:
30.06.93 Bulletin 93/26

(84) Designated Contracting States:
DE GB

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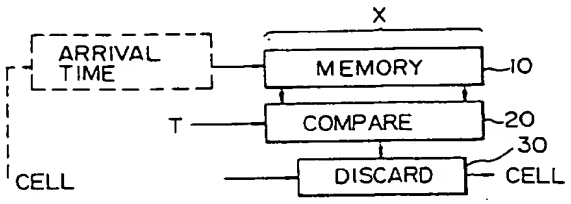
(54) Usage parameter control circuit.

(57) A usage parameter control circuit for effecting a policing control in an ATM transmission network, comprising a time interval measuring unit (10) for measuring a time interval between a currently arrival time of a cell to be judged, and an arrival time of a cell which arrived a reference threshold number (X) of cells before the currently arriving cell arrives; and a judging unit (20) for judging whether or not the measured time interval is shorter than a reference threshold time interval (T), whereby a longer accessing time is allowed and the circuit construction has a flexible expandability.

Fig. 2



EP 0 548 995 A2

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a usage parameter control (UPC) circuit for controlling a flow amount of cells based on reference threshold information relating to cell traffic.

As a basic technology for a Broadband Aspects of Integrated Services Digital Network (B-ISDN), an Asynchronous Transfer Mode (ATM) technology for asynchronously transferring cells has been developed. In the ATM network, the amount of cell flow is controlled based on traffic parameters declared by subscribers. This control is called a policing control or a Usage Parameter Control (UPC) which is an essential technology for smooth operation of the ATM network. The user declaration traffic parameters, however, are different depending on the subscribers. This difference makes it difficult to realize a UPC circuit.

(2) Description of the Related Art

As a conventional policing control method, a time interval method has been proposed in which the cell transmission is controlled by counting cell arrival time intervals for respective cells and by comparing each time interval with a reference threshold time.

Another conventional policing method has been proposed as a T-X method in which the number of cells arriving within a reference threshold time period are measured and the number is compared with a reference threshold value to control the cell transmission.

Still another conventional method has been proposed as a dangerous bridge (DB) method in which the number of cells arriving during a reference threshold time are counted while the starting time point of the reference threshold time period is shifted by one cell transmission time at the time of each counting operation, and the counted number is compared with a reference threshold number of cells, to control the cell transmission.

In the time interval method, the cell arrival time interval is determined for each cell so that there is a small amount of flexibility in the continuous control of cell speed.

The T-X method has a large amount of flexibility in the continuous control of cell speed, however, when cells are concentrated at a boundary region of the reference threshold time period, these cells cannot be efficiently restricted.

In the conventional DB method, a plurality of taps in a bridge memory must be accessed each time a cell arrives. This simultaneous access of plural taps is difficult to realize because the memory access time is restricted to a certain period. In addition, there is another problem in the conventional DB method in that, if a software error is generated in a memory or in a counter, the error does not disappear within a limited time period.

Accordingly, in the conventional UPC circuit, since the parameters declared by subscribers are different depending on the subscribers, and if all of the parameters are to be taken into consideration, the conventional UPC circuit has a disadvantage of being too complex and requiring large hardware.

An object of the present invention is to provide a new UPC circuit having a simple traffic judgement unit as a construction unit and being superior in general purpose characteristics and flexible expandability.

SUMMARY OF THE INVENTION

To attain the above object, there is provided, according to the present invention, a usage parameter control circuit for effecting a policing control in an ATM transmission network to restrict transmission of an arriving cell when the arriving cell is in violation of at least one of usage parameters declared by a subscriber, comprising: a time interval measuring unit for measuring a time interval between a currently arriving time of a cell to be judged as to whether or not the cell is in violation, and an arrival time of a cell which arrived a reference threshold number of cells before the currently arriving cell arrives; and a judging unit for judging whether or not the measured time interval is shorter than a reference threshold time interval, the reference threshold number of cells and the reference threshold time interval being at least a part of the usage parameters declared by the subscriber, the currently arriving cell being judged to be in violation of the usage parameters when the measured time interval is shorter than the predetermined time interval.

According to an aspect of the present invention, the time interval measuring unit comprises a memory for storing the arrival time of the cell which arrived the reference threshold number of cells before the currently arriving cell arrives; and the usage parameter control circuit further comprises a cell discarding unit; the judging unit judging, based on the judgement of whether or not the measured time interval is shorter than the reference threshold time interval, whether or not the number of cells passed within the reference threshold time interval is larger than the reference threshold number of cells; and the cell discarding unit discarding the currently arriving cell when the judging unit judges that the number of cells passed within the reference threshold time interval is larger than the reference threshold number of cells.

According to another aspect of the present invention, the time interval measuring unit comprises; a bridge memory for storing, in a time sequence, at least one cell type of cells arriving at the input of the bridge memory; and a first pointer holding unit for holding a first pointer indicating a storing position of a cell type, stored in the bridge memory, of a cell, the stored cell type being the same as the cell type of an arriving cell to be judged; and the judging unit comprises a control unit for judging whether or not an arriving cell to be judged is in violation by controlling the bridge memory and the first pointer holding unit.

Preferably, the control unit comprises a comparing unit for comparing the time interval determined, each time a cell to be judged arrives at the input of the bridge memory, by a difference between the storing position indicated by the first pointer holding unit and the input position of the bridge memory with the reference threshold time interval, whereby the arriving cell is judged to be in violation when the measured time interval is shorter than the reference threshold time interval.

Preferably, when the control unit judges that the arriving cell is not in violation, the control unit controls the first pointer holding unit to store the position information of the cell type of the arriving cell at the input of the bridge memory.

Preferably, the usage parameter control circuit further comprises a counting unit for counting the number of cell types or cells, the cell types being stored in the bridge memory, the cell types of the cells being the same as the cell type of an arriving cell to be judged; the control unit controlling the counting unit to count the number of cell types of the cells up to a certain number n from a cell type at the input of the bridge memory (BM) to an already stored cell type.

Preferably, the certain number n is a reference threshold number of cells declared by a subscriber.

Preferably, when the count value of the counting unit is smaller than the certain number n each time a cell to be judged arrives, the control unit judges that the arriving cell is not in violation.

Preferably, the control unit controls the first pointer holding unit to store the storing position of the cell type of a cell that arrived the number indicated by the counting unit before the currently arriving cell, the cell type being the same as the cell type of a currently arriving cell to be judged.

Preferably, the bridge memory comprises: cell type storing areas for storing cell types; and next pointer storing areas respectively related to the cell type storing areas, each of the next pointer storing areas storing a position of a cell type of a cell which arrived next to the arrival of the cell type stored in the related cell type storing area, the control unit chaining together a plurality of the cell type storing areas of cells, having the same cell type as the cell type of a currently arriving cell to be judged, by using the next pointer storing areas.

Preferably, the circuit further comprises a last pointer holding unit for holding the storing position of a cell type of a cell which is most-recently stored in the bridge memory, the cell type being the same as the cell type of the currently arriving cell to be judged; the control unit controlling, when an arriving cell is judged not to be in violation, the last pointer holding unit so as to store the position information of the input of the bridge memory into the next pointer storing area corresponding to the position stored in the last pointer holding unit.

Preferably, when the count value of the counting unit is n when a cell to be judged arrives, the control unit controls the first pointer holding unit to record the information stored in the next pointer storing area indicated by the first pointer holding unit in the bridge memory into the first pointer holding unit.

Preferably, the bridge memory comprises at least one flag storing area corresponding to the cell type storing area, the control unit controlling the storing area in the bridge memory to be valid or invalid by using the flag storing area.

Preferably, the control circuit forcedly changes the contents of the flag storing area in a storing position, which is to be shifted, at the next timing, to the input of the bridge memory, to be invalid.

Preferably, the control circuit forcedly changes the contents of the flag storing area of a cell to be judged, which arrived before arriving the cell at the position indicated by the first pointer holding unit, to be invalid.

Preferably, the control circuit uses a plurality of the flag storing areas to perform a plurality of policing judgements.

Preferably, the first pointer holding units are provided to respectively correspond to cell types.

Preferably, the counting unit are provided to respectively correspond to the cell types.

Preferably, the last pointer holding units are provided to respectively correspond to the cell types.

Preferably, the first pointer holding units are included in a random access memory.

Preferably, the counting units are included in a random access memory.

Preferably, the first pointer holding units are included in a random access memory.

Preferably, the bridge memory is constructed by a random access memory which operates as a first-in first-out memory.

Preferably, the bridge memory stores a plurality of kinds of the cell type information.

Preferably, the storing capacity of the bridge memory (BM) is selected from one of a Tmax,

Tmax + 1, and 2^k (where k is a natural number) that is the minimum value larger than Tmax, where Tmax is the maximum value of reference threshold time intervals of plural cell types.

Preferably, the control unit comprises a hardware error detecting unit for detecting a hardware error by detecting that the count value of the counting unit is negative or larger than the number n.

Preferably, the control unit comprises a hardware error detecting unit for detecting a hardware error by detecting that, when the bridge memory is accessed by the first pointer holding unit or the last pointer holding unit, the control unit acknowledges the cell type of the cell at the accessed storing position.

Preferably, when a hardware error is detected, the control unit resets the counting unit and makes at least the flag storing areas in the bridge memory invalid.

Preferably, the counting unit is periodically reset, and at least the flag storing areas in the bridge memory are periodically made invalid.

Preferably, when the counting unit is reset, the policing process for arriving cells is not performed for a predetermined time period.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and other features of the present invention will be more apparent from the following description of the preferred embodiment with reference to the drawings, wherein:

Fig. 1 is a diagram explaining the principle of the first embodiment of the present invention;

Fig. 2 is a block diagram explaining the principle of the first embodiment of the present invention;

Fig. 3 is a block diagram showing a usage policing control circuit according to the first embodiment of the present invention;

Fig. 4 is a block diagram showing a modification of the UPC circuit shown in Fig. 3;

Fig. 5 is a block diagram showing a modification of the UPC circuit shown in Fig. 3;

Fig. 6 is a block diagram showing a modification of the UPC circuit shown in Fig. 3;

Fig. 7 is a block diagram showing in detail the UPC circuit shown in Fig. 3;

Fig. 8A is a block diagram explaining the principle of the second embodiment of the present invention;

Figs. 8B and 8C are diagrams explaining the operation of the circuit shown in Fig. 8A;

Fig. 9A is a block diagram showing a UPC circuit according to the second embodiment of the present invention;

Fig. 9B is a diagram showing an example of the contents of the bridge memory shown in Fig. 9A;

Fig. 10 is a flowchart explaining a judgement process in the UPC circuit shown in Fig. 9A;

Fig. 11 is a flowchart explaining a pointer process in the UPC circuit shown in Fig. 9A;

Fig. 12 is a flowchart explaining a shift process in the UPC circuit shown in Fig. 9A;

Figs. 13 A to 13C are diagrams explaining a part of the operation of the UPC circuit shown in Fig. 9A;

Figs. 14A to 14C are diagrams explaining another part of the operation of the UPC circuit shown in Fig. 9A;

Figs. 15A to 15C are diagrams explaining still another part of the operation of the UPC circuit shown in Fig. 9A;

Fig. 16A to 16C are diagrams explaining still another part of the operation of the UPC circuit shown in Fig. 9A;

Figs. 17A to 17C are diagrams explaining still another part of the operation of the UPC circuit shown in Fig. 9A;

Figs. 18A and 18B are flowcharts explaining a modification of the judgement process in the UPC circuit shown in Fig. 9A;

Figs. 19A and 19B are flowcharts explaining a modification of the pointer process in the UPC circuit shown in Fig. 9A;

Fig. 20 is a flowchart explaining the error process in the UPC circuit shown in Fig. 9A;

Fig. 21 is a block diagram of an UPC circuit according to the third embodiment of the present invention;

Fig. 22 is a flowchart explaining the judgement process in the UPC circuit shown in Fig. 21;

Fig. 23 is a flowchart explaining the pointer process in the UPC circuit shown in Fig. 21;

Fig. 24 is a flowchart explaining the shift process in the UPC circuit shown in Fig. 21;

Figs. 25A to 25C are diagrams explaining a part of the operation of the UPC circuit shown in Fig. 21;

Figs. 26A to 26C are diagrams explaining another part of the operation of the UPC circuit shown in Fig. 21;

Figs. 27A to 27C are diagrams explaining still another part of the operation of the UPC circuit shown in Fig. 21;

Fig. 28A is a diagram showing ATM cells on a transmission line for explaining the background of the present invention;

Fig. 28B is a diagram explaining a basic structure of the ATM packet for explaining the background of the present invention;

Fig. 29 is a diagram explaining a time interval method proposed prior to the present invention;

Fig. 30 is a diagram explaining a T-X method proposed prior to the present invention;

Fig. 31 is a diagram explaining a DB method proposed prior to the present invention; and
Fig. 32 is a block diagram showing a conventional UPC circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

For better understanding of the present invention, the background and the technologies proposed before the present invention will first be described with reference to Figs. 28A to 32.

Fig. 28A shows ATM cells on a transmission line. Each ATM cell consists of a header part (5 bytes) and a data part (48 bytes). The subscriber side of the transmission line is connected to a sound terminal such as a telephone terminal, a visual terminal such as a television terminal, a facsimile terminal, a data communication terminal, an inter-LAN connection terminal, or so on.

Fig. 28B shows the basic structure of the ATM cell. As shown in Fig. 28B, the ATM cell is constructed of the header of 5 bytes and a payload of 48 bytes comprising a fixed length packet, which is asynchronously transmitted through various nodes, i.e., through a path between cross-connect units in an ATM transmission network. By the ATM transmission, only when information to be sent is generated, is a fixed length packet (hereinafter referred to as a cell) transmitted. Therefore, the efficiency of use of the line is high, and all kinds of data rates can be handled by one technology. Accordingly, in the ATM transmission network, it is not necessary to allocate a time slot so that the ATM transmission network is suitable for a dispersion process control and is flexibly adapted to a multiplexed transmission in comparison with a synchronous transfer mode (STM).

When such an ATM transmission network is used for a subscriber system, if subscribers are allowed to freely transmit a cell, imbalance is generated among the subscribers depending on the frequency of the generation of the information. To prevent the imbalance, a contract is made between a supplier of the network located in each node and a subscriber with respect to an upper limit of the cells which can be transmitted within a unit time so that each subscriber transmits cells in accordance with the contract, and the supplier of the network checks, at the input of the network, whether or not the subscriber is transmitting the cells within the scope of the contract, so as to protect the network. This checking function is called policing control.

Figs. 29 to 31 are diagrams for explaining the already proposed policing control methods prior to the present invention.

Fig. 29 shows a time interval method in which a time interval t between adjacent arrival cells is counted by a counter circuit, and the time t is compared with a reference threshold time period T to judge the amount of flowing cells.

By the time interval method shown in Fig. 29, the time interval is restricted for each cell so that there is a small amount of flexibility in the continuous control of cell speed.

Fig. 30 shows a T-X method in which the number of cells x arriving during a reference threshold time period T is counted by a counter circuit, and the number x is compared with a reference threshold number X to judge the amount of flowing cells.

The T-X method shown in Fig. 30 has a large amount of flexibility in the continuous control of cell speed, however, when cells are concentrated at a boundary region of the reference threshold time period, these cells cannot be efficiently restricted.

Fig. 31 shows a dangerous bridge (DB) method in which each reference threshold time period T is shifted by one cell passing time period Δ t. Within each reference threshold time period T, the number x of arriving cells is counted by a counter circuit, and the number x is compared with a reference threshold number X to judge the amount of flowing cells.

Fig. 32 is a block diagram showing a conventional UPC circuit employing a DB-BM (DB-Bridge Memory) method. In the figure, 100 is a cell, 101 is a header part, 102 is a payload (data) part, 1 is a cell information branching unit (SB), 2 is a cell delaying unit (SM), 3 is a cell control unit (SC), 21 is a bridge memory (BM) having a T_{max} -length shift register, 22 is a multi-tap circuit (TAP), 23_0 to 23_m are judging units, SF in each judging unit is a cell filter for passing a particular one of header information VP_0, ..., and VP_m , CTR is a counter circuit which operates with an up/down mode, CMP is a comparator, PM is a parameter memory for storing a declared parameter X_0, ..., or X_m.

When a cell arrives at an input of the highway, the header information VP in the cell is branched or copied by the cell information branching unit 1 and is temporarily stored in the cell delaying unit 2. On the other hand, the bridge memory 21 stores the branched header information VP in a time sequence. The multi-tap circuit 22 reads, from the bridge memory 21 of T_{max} length, the header information VP which is delayed by a time corresponding to the time value T_0, ..., or T_m declared by the subscriber, and supplies the read header information VP to the corresponding judging unit 23_0, ..., or 23_m.

The disadvantage of the above conventional UPC circuit is that it includes the multi-tap circuit 22 so that the wirings for the multi-tap circuit 22 are large. In addition, it is not easy to change the tap positions.

It should be noted that the policing control in accordance with the peak value and the policing control in accordance with the average value may be executed simultaneously. In this case, in the above example, in the control according to the average value, up to three cells are allowed to pass within the reference threshold time interval AT = 6, while, in the control according to the peak value simultaneously executed with the control according to the average value, the continuous three cells are not allowed to pass within the reference threshold time interval PT = 3.

In the above-described third embodiment of the present invention, with respect to the cell with the cell type information $\bar{a}$ which was actually discarded in the peak value control, the cell is judged not to be in violation in the average value control and the cell type information $\bar{a}$ is stored in the bridge memory (BM) 94a. The present invention, however, is not restricted to this. For example, with respect to the cell with the cell type information $\bar{a}$ which was actually discarded in the peak value control, the cell may be forcedly treated as a violating cell or it may be assumed that the cell with the information $\bar{a}$ has not arrived. A similar discussion can be applied with respect to the cell which was actually discarded in the peak value control. In these cases, it is not necessary to provide a plurality of last pointers such as the PLP and ALP, but a single last pointer common to the average value control and the peak value control.

In the above embodiments, all of the counter memories CM are reset when a hardware error is detected or periodically, and at least the flag storing areas F are made invalid, however, the present invention is not restricted to this. For example, there is a case in which it is possible to recover the UPC circuit from an abnormal state by resetting the counter memories CM corresponding to a particular cell type, and by making the flag storing areas F corresponding to the cell types.

In the above described embodiment, with respect to a cell having a predetermined cell type, the policing judgement according to the average value declaration and the policing judgement according to the peak value declaration are described. The present invention, however, is not restricted to these. There may be three or more kinds of flags, and these flags may be freely used for any control system having any object.

In the above embodiments, the control unit CTL shown in Fig. 8A or the CPU 96 is operated by software, however, the control unit CTL or the CPU 96 and the ROM 97 may be formed by hardware.

From the foregoing description, it will be apparent that, according to the present invention, the memory accessing speed can be greatly decreased so that the policing control according to the dangerous bridge method can be realized. In addition, the influence of a software error in a memory can be removed within a limited time. Still further, by providing a bridge memory for storing cell type information of arriving cells in a time sequence, a first pointer holding means for holding the storing positions of the cell type information of the cells to be judged, and a control unit for controlling them to execute a policing judgement, a simple traffic judging unit is realized so that a down-sized UPC circuit being superior in general purpose characteristics and flexible expandability can be provided.

Claims

1. A usage parameter control circuit for effecting a policing control in an ATM transmission network to restrict transmission of an arriving cell when the arriving cell is in violation of at least one of usage parameters declared by a subscriber, comprising:

   time interval measuring means (10) for measuring a time interval between a currently arrival time of a cell to be judged as to whether or not the cell is in violation, and an arrival time of a cell which arrived a reference threshold number (X) of cells before the currently arriving cell arrives; and

   judging means (20) for judging whether or not the measured time interval is shorter than a reference threshold time interval (T), said reference threshold number of cells and said reference threshold time interval (T) being at least a part of said usage parameters declared by the subscriber, the currently arriving cell being judged to be in violation of the usage parameters when the measured time interval is shorter than the predetermined time interval (T).

2. A usage parameter control circuit as claimed in claim 1, wherein said time interval measuring means comprises a memory (10) for storing the arrival time of the cell which arrived the reference threshold number (X) of cells before the currently arriving cell arrives; and the usage parameter control circuit further comprises cell discarding means (30);

   said judging means (20) judging, based on the judgement of whether or not the measured time interval is shorter than the reference threshold time interval (T), whether or not the number of cells passed within the reference threshold time interval (T) is larger than the reference threshold number of cells; and

   said cell discarding means (30) discarding

the currently arriving cell when said judging means judges that the number of cells passed within the reference threshold time interval (T) is larger than the reference threshold number of cells.

3. A usage parameter control circuit as claimed in claim 2, wherein said memory (10) is a logical shift register constructed by a random access memory and pointers for indicating the addresses of said random access memory.

4. A usage parameter control circuit as claimed in claim 3, further comprising write inhibit means for inhibiting the writing of the currently arrival time into said memory (10) when said cell discarding means discards the currently arriving cell.

5. A usage parameter control circuit as claimed in claim 1, further comprising :

adjacent cell time interval measuring means (11, 12) for measuring an arrival time interval between adjacent cells each time a cell to be judged arrives;

a memory (10) for storing the arrival time interval between adjacent cells each time a cell to be judged arrives; and

cell discarding means (30);

the measured time interval between a currently arrival time of a cell to be judged and an arrival time of a cell which arrived a reference threshold number (X) of cells before the currently arriving cell arrives being obtained by adding the reference threshold number (X) of the arrival time intervals stored in the memory (10);

said judging means (20) judging, based on the judgement of whether or not the measured time interval is shorter than the reference threshold time interval (T), whether or not the number of cells passed within the reference threshold time interval (T) is larger than the reference threshold number of cells; and

said cell discarding means (30) discarding the currently arriving cell when said judging means judges that the number of cells passed within the reference threshold time interval (T) is larger than the reference threshold number of cells.

6. A usage parameter control circuit as claimed in claim 5, wherein said memory (10) is a logical shift register constructed by a random access memory and pointers for indicating the addresses of said random access memory.

7. A usage parameter control circuit as claimed in claim 6, further comprising write inhibit means for inhibiting the writing of the arrival time interval into said memory (10) when said cell discarding means discards the currently arriving cell.

8. A usage parameter control circuit as claimed in claim 5, wherein the adjacent cell time interval measuring means comprises a timer counter (6) provided to correspond to each cell type information, for counting a time, the count value in the timer counter being input to the memory each time when a cell arrives at the input of the memory, and the count value of the timer counter being reset each time the count value is input to the memory (10).

9. A usage parameter control circuit as claimed in any one of claims 2 to 8, wherein said memory (10) is provided to correspond to each cell type information.

10. A usage parameter control circuit as claimed in claim 9, wherein at least one of said reference threshold time interval (T) and said reference threshold number (X) depends on the cell type information.

11. A usage parameter control circuit for effecting a policing control in an ATM transmission network to restrict the transmission of an arriving cell when the arriving cell is in violation of at least one of usage parameters declared by subscribers, comprising:

a plurality of judging units (42_0, ..., 42_m) provided to respectively correspond to cell types, each for judging whether or not an arriving cell of a corresponding cell type is in violation of corresponding usage parameters declared by a subscriber;

each of the judging units comprising:

time interval measuring means (10) for measuring a time interval between a currently arrival time of a cell to be judged as to whether or not the cell is in violation, and an arrival time of a cell which arrived a reference threshold number (X) of cells before the currently arriving cell arrives; and

judging means (20) for judging whether or not the measured time interval is shorter than a reference threshold time interval (T), said reference threshold number of cells and said reference threshold time interval (T) being at least a part of said usage parameters declared by the subscriber, the currently arriving cell being judged to be in violation of the usage parameters when the measured time interval is

shorter than the predetermined time interval (T).

12. A usage parameter control circuit as claimed in claim 1, wherein said time interval measuring means (10) comprises;

a bridge memory (BM) for storing, in a time sequence, at least one cell type of cells arriving at the input of the bridge memory; and

first pointer holding means (XP) for holding a first pointer indicating a storing position of a cell type, stored in the bridge memory, of a cell, the stored cell type being the same as the cell type of an arriving cell to be judged; and

said judging means comprises a control unit (CTL) for judging whether or not an arriving cell to be judged is in violation by controlling the bridge memory (BM) and the first pointer holding means (XP).

13. A usage parameter control circuit as claimed in claim 12, wherein said control unit (CTL) comprises comparing means for comparing the time interval determined, each time a cell to be judged arrives at the input of the bridge memory (BM), by a difference between the storing position indicated by said first pointer holding means and the input position of the bridge memory with the reference threshold time interval (T), whereby the arriving cell is judged to be in violation when the measured time interval is shorter than the reference threshold time interval (T).

14. A usage parameter control circuit as claimed in claim 13, wherein when the control unit (CTL) judges that the arriving cell is not in violation, the control unit (CTL) controls the first pointer holding means (XP) to store the position information of the cell type of the arriving cell at the input of the bridge memory (BM).

15. A usage parameter control circuit as claimed in claim 13, further comprising counting means (CM) for counting the number of cell types or cells, the cell types being stored in the bridge memory (BM), the cell types of the cells being the same as the cell type of an arriving cell to be judged;

the control unit (CTL) controlling the counting means (CM) to count the number of cell types of the cells up to a certain number n from a cell type at the input of the bridge memory (BM) to an already stored cell type.

16. A usage parameter control circuit as claimed in claim 15, wherein the certain number n is a reference threshold number (X) of cells declared by a subscriber.

17. A usage parameter control circuit as claimed in claim 15, wherein when the count value of the counting means (CM) is smaller than the certain number n each time a cell to be judged arrives, the control unit (CTL) judges that the arriving cell is not in violation.

18. A usage parameter control circuit as claimed in claim 15, wherein the control unit (CTL) controls the first pointer holding means (XP) to store the storing position of the cell type of a cell that arrived the number indicated by the counting means (CM) before arriving the currently arriving cell, the cell type being the same as the cell type of a currently arriving cell to be judged.

19. A usage parameter control circuit as claimed in claim 18, wherein the bridge memory (BM) comprises:

cell type storing areas (VP) for storing cell types; and

next pointer storing areas (NP) respectively related to the cell type storing areas (VP), each of the next pointer storing areas (NP) storing a position of a cell type of a cell which arrived next to the arrival of the cell type stored in the related cell type storing area (VP), the control unit (CTL) chains together a plurality of the cell type storing areas of cells, having the same cell type as the cell type of a currently arriving cell to be judged, by using the next pointer storing areas (NP).

20. A usage parameter control circuit as claimed in claim 19, further comprising:

last pointer holding means (LP) for holding the storing position of a cell type of a cell which is most-recently stored in the bridge memory (BM), the cell type being the same as the cell type of the currently arriving cell to be judged;

the control unit (CTL) controlling, when an arriving cell is judged not to be in violation, the last pointer holding means (LP) so as to store the position information of the input of the bridge memory (BM) into the next pointer storing area corresponding to the position stored in the last pointer holding means (LP).

21. A usage parameter control circuit as claimed in claim 20, wherein when the count value of the counting means (CM) is n when a cell to be judged arrives, the control unit (CTL) controls the first pointer holding means (XP) to record the information stored in the next pointer stor-

ing area (NP) indicated by the first pointer holding means (XP) in the bridge memory (BM) into the first pointer holding means (XP).

22. A usage parameter control circuit as claimed in claim 21, wherein the bridge memory comprises at least one flag storing area (F) corresponding to the cell type storing area (VP), the control unit (CTL) controlling the storing area in the bridge memory (BM) to be valid or invalid by using the flag storing area (F).

23. A usage parameter control circuit as claimed in claim 22, wherein the control circuit (CTL) forcedly changes the contents of the flag storing area (F) in a storing position, which is to be shifted, at the next timing, to the input of the bridge memory (BM), to be invalid.

24. A usage parameter control circuit as claimed in claim 22, wherein the control circuit (CTL) forcedly changes the contents of the flag storing area (F) of a cell to be judged, which arrived before arriving the cell at the position indicated by the first pointer holding means (XP), to be invalid.

25. A usage parameter control circuit as claimed in claim 22, wherein the control circuit (CTL) uses a plurality of the flag storing areas (F) to perform a plurality of policing judgements.

26. A usage parameter control circuit as claimed in claim 12, wherein the first pointer holding means (XP) are provided to respectively correspond to cell types.

27. A usage parameter control circuit as claimed in claim 15, wherein the counting means (CM) is provided to respectively correspond to the cell types.

28. A usage parameter control circuit as claimed in claim 20, wherein the last pointer holding means is provided to respectively correspond to the cell types.

29. A usage parameter control circuit as claimed in claim 26, wherein the first pointer holding means (XP) is included in a random access memory.

30. A usage parameter control circuit as claimed in claim 27, wherein the counting means (CM) is included in a random access memory.

31. A usage parameter control circuit as claimed in claim 28, wherein the first pointer holding means (XP) is included in a random access memory.

32. A usage parameter control circuit as claimed in claim 12, wherein the bridge memory (BM) is constructed by a random access memory which operates as a first-in first-out memory.

33. A usage parameter control circuit as claimed in claim 12, wherein the bridge memory (BM) stores a plurality of kinds of the cell type information.

34. A usage parameter control circuit as claimed in claim 12, wherein the storing capacity of the bridge memory (BM) is selected from one of a Tmax, Tmax + 1, and 2^k (where k is a natural number) that is the minimum value larger than Tmax, where Tmax is the maximum value of reference threshold time intervals of plural cell types.

35. A usage parameter control circuit as claimed in claim 22, wherein the control unit (CTL) comprises hardware error detecting means for detecting a hardware error by detecting that the count value of the counting means (CM) is negative or larger than the number n.

36. A usage parameter control circuit as claimed in claim 22, wherein the control unit (CTL) comprises hardware error detecting means for detecting a hardware error by detecting that, when the bridge memory (BM) is accessed by the first pointer holding means (XP) or the last pointer holding means (LP), the control unit (CTL) acknowledges the cell type of the cell at the accessed storing position.

37. A usage parameter control circuit as claimed in claim 35 or 36, wherein when a hardware error is detected, the control unit (CTL) resets the counting means (CM) and makes at least the flag storing areas (F) in the bridge memory (BM) to be invalid.

38. A usage parameter control circuit as claimed in claim 22, wherein the counting means (CM) is periodically reset, and at least the flag storing areas (F) in the bridge memory (BM) are periodically made invalid.

39. A usage parameter control circuit as claimed in claim 37 or 38, wherein when the counting means (CM) is reset, the policing process for arriving cells is not performed for a predetermined time period.

Fig. 1

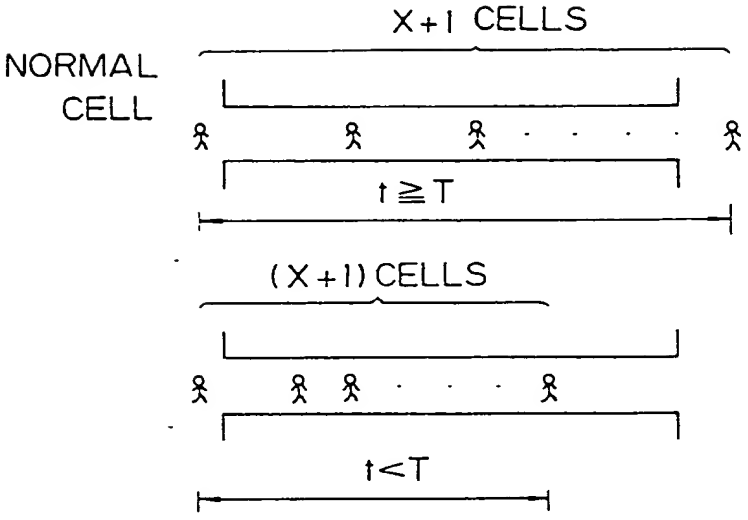

X+1 CELLS
NORMAL CELL
t ≧ T
(X+1) CELLS
t<T

Fig. 2

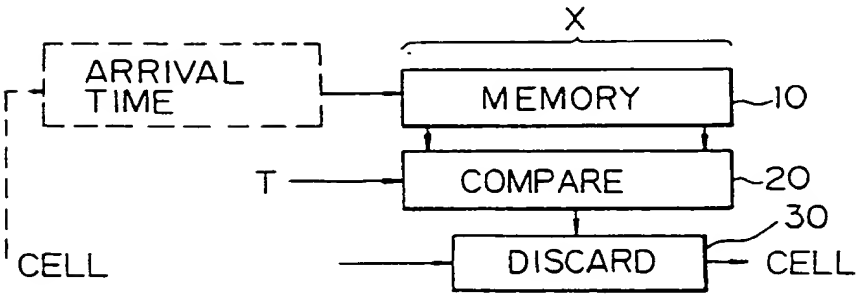

X
ARRIVAL TIME
MEMORY
10
T
COMPARE
20
30
CELL
DISCARD
CELL

Fig. 3

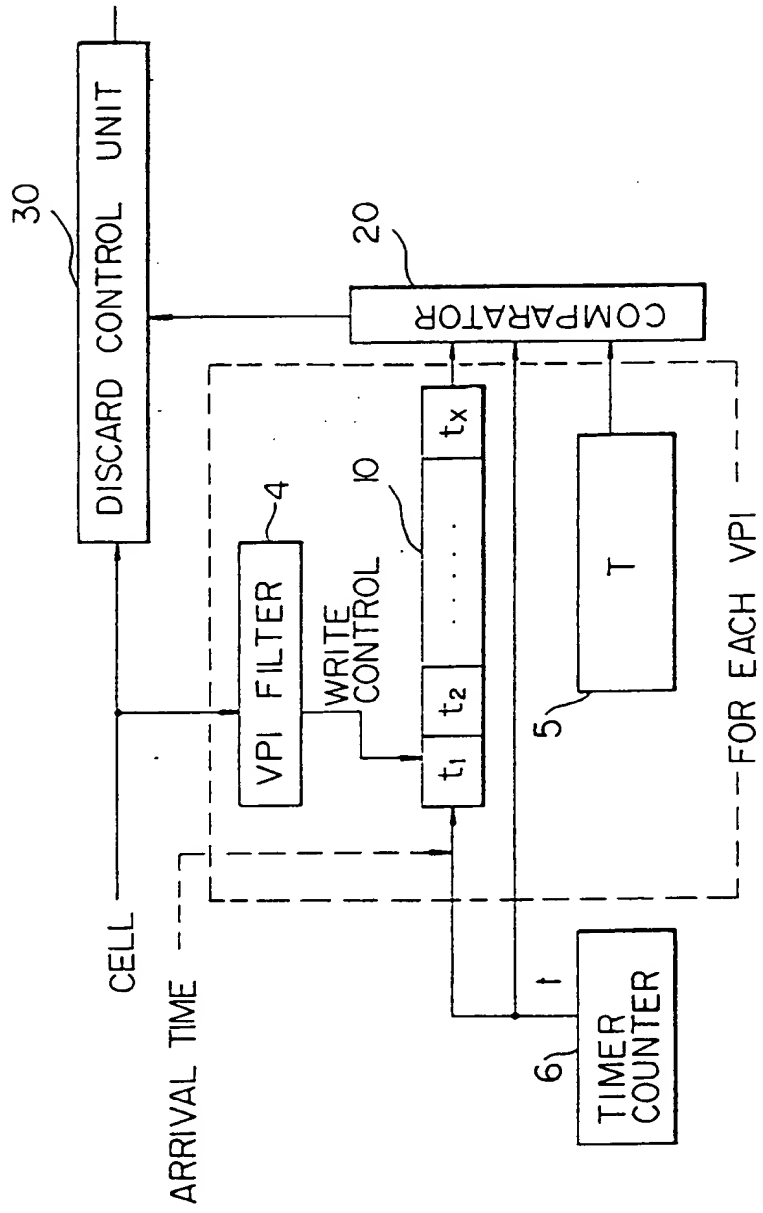

30
DISCARD CONTROL UNIT
20
COMPARATOR
4
VPI FILTER
WRITE CONTROL
10
t_x
t_2
t_1
T
5
FOR EACH VPI
CELL
ARRIVAL TIME
t
6
TIMER COUNTER

Fig. 4

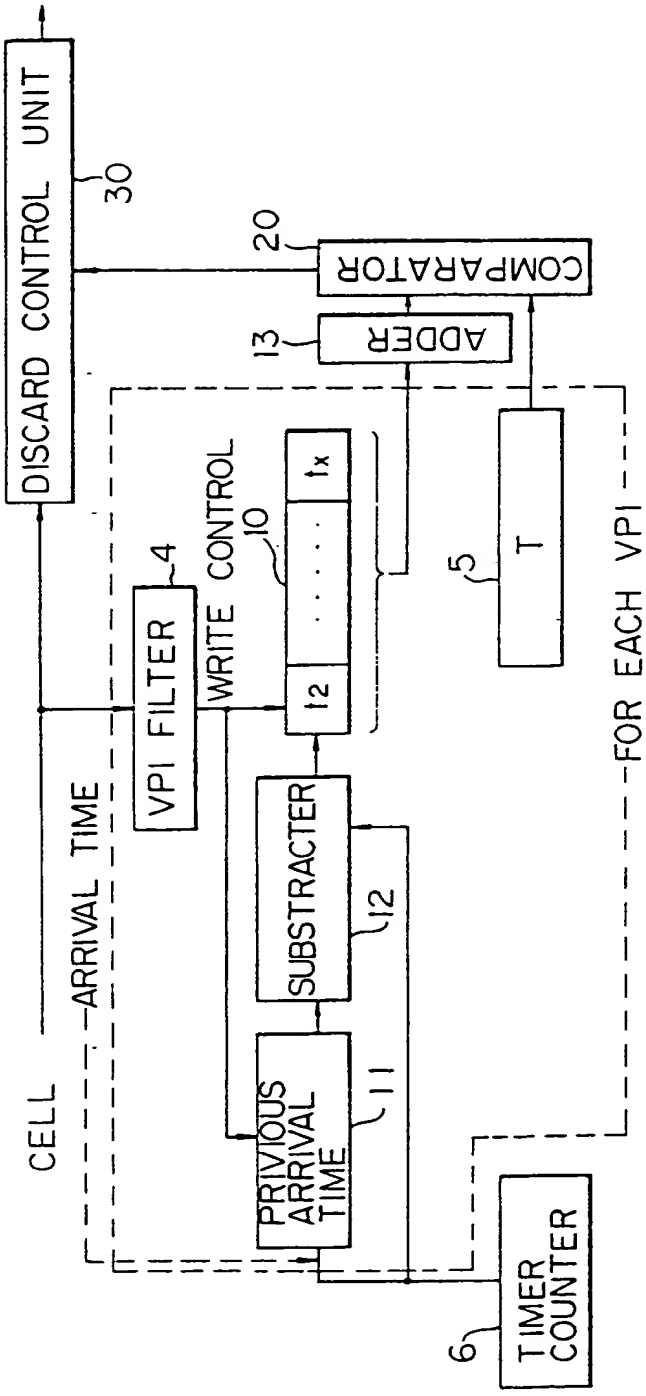

DISCARD CONTROL UNIT
30
20
COMPARATOR
13
ADDER
T
5
tx
t2
WRITE CONTROL
10
VPI FILTER
4
SUBSTRACTER
12
PRIVIOUS ARRIVAL TIME
11
TIMER COUNTER
6
CELL
ARRIVAL TIME
FOR EACH VPI

Fig. 5

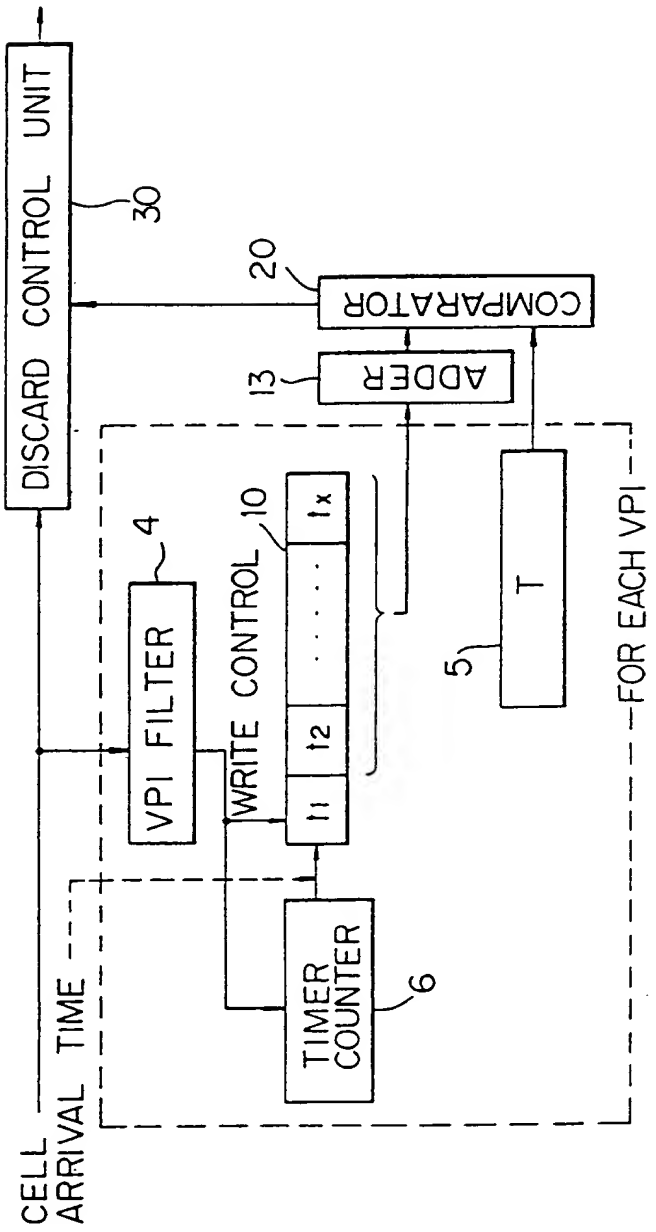

DISCARD CONTROL UNIT
30
20
COMPARATOR
13
ADDER
4
VPI FILTER
10
WRITE CONTROL
t1
t2
tx
5
T
FOR EACH VPI
CELL ARRIVAL TIME
TIMER COUNTER
6

Fig. 6

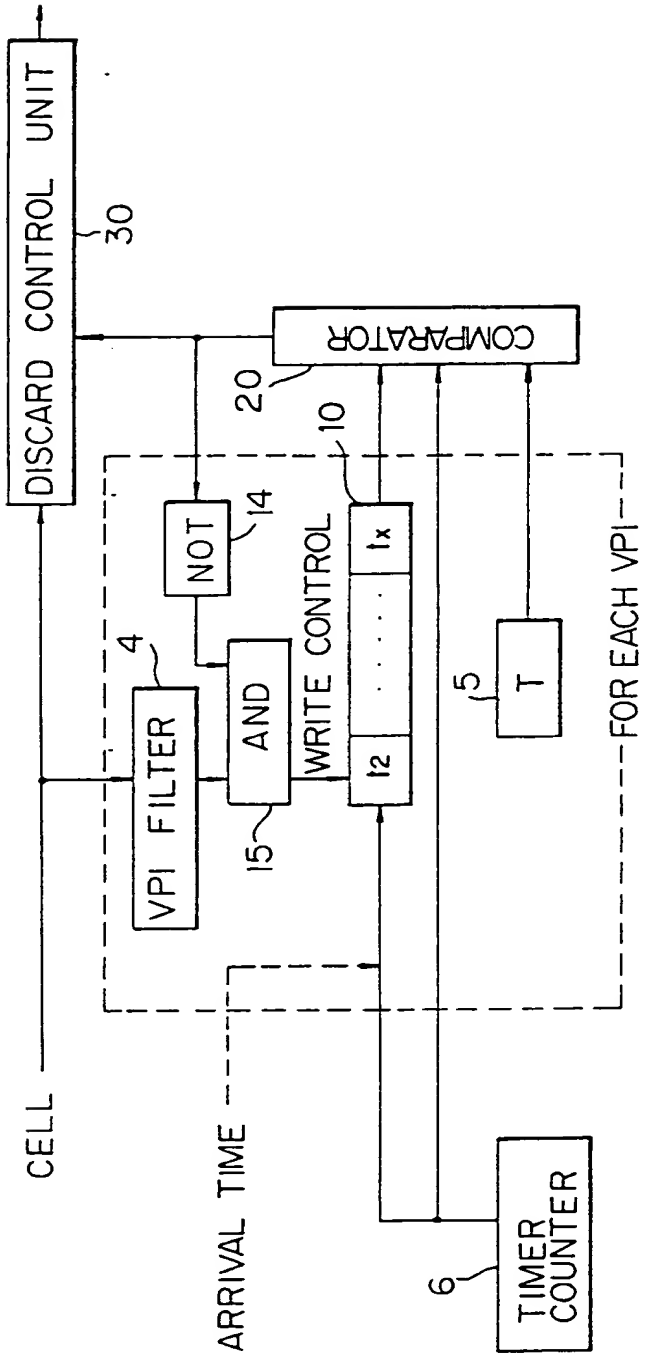

DISCARD CONTROL UNIT
30
COMPARATOR
20
10
NOT
14
AND
15
4
VPI FILTER
WRITE CONTROL
1x
12
5
T
FOR EACH VPI
CELL
ARRIVAL TIME
6
TIMER COUNTER

Fig. 7

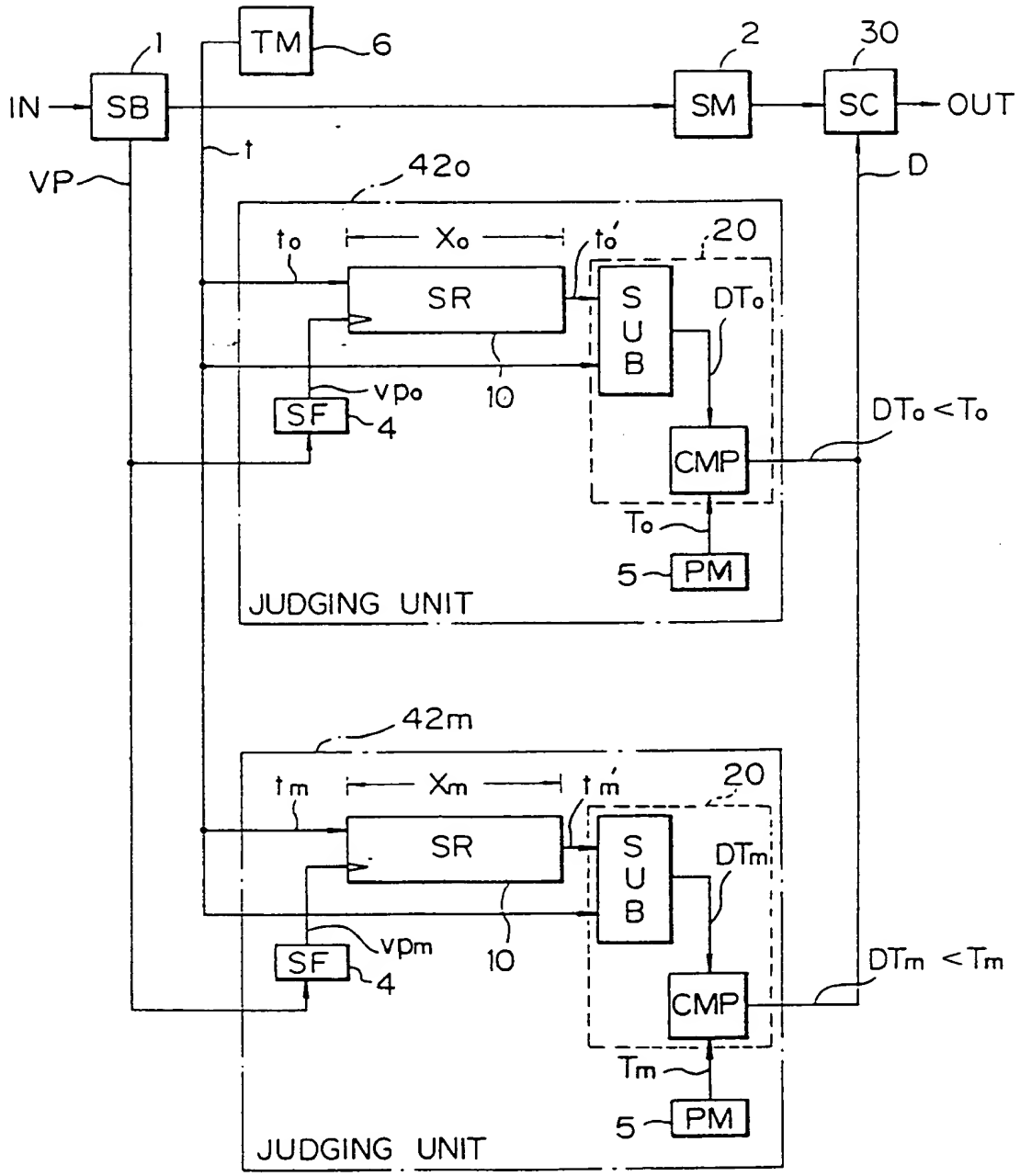

IN
SB
1
TM
6
SM
2
SC
30
OUT
VP
t
D
42o
to
Xo
to'
20
SR
SUB
DTo
vpo
10
SF
4
DTo <To
CMP
To
5
PM
JUDGING UNIT
42m
tm
Xm
tm'
20
SR
SUB
DTm
vpm
10
SF
4
DTm <Tm
CMP
Tm
5
PM
JUDGING UNIT

Fig. 8A

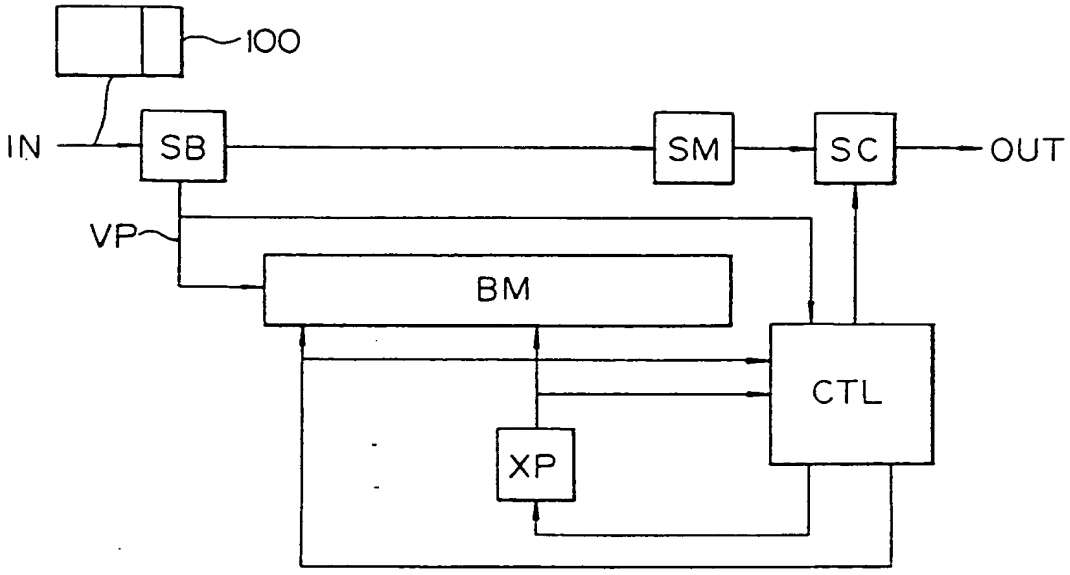


Fig. 8B

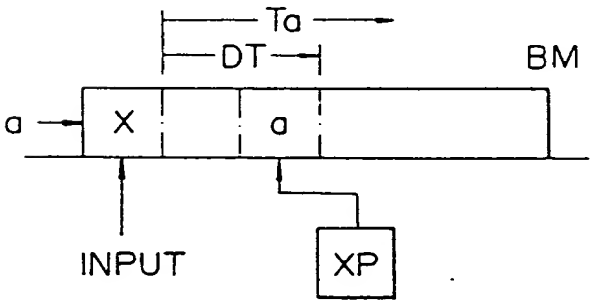


Fig. 8C

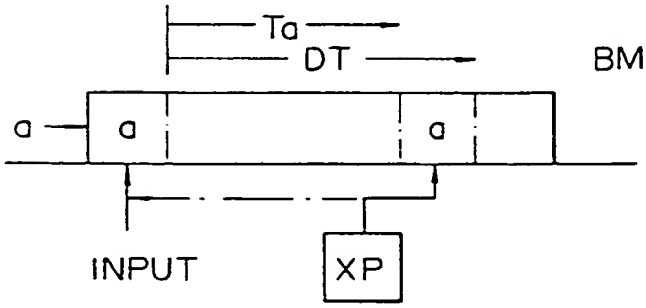


Fig. 9A

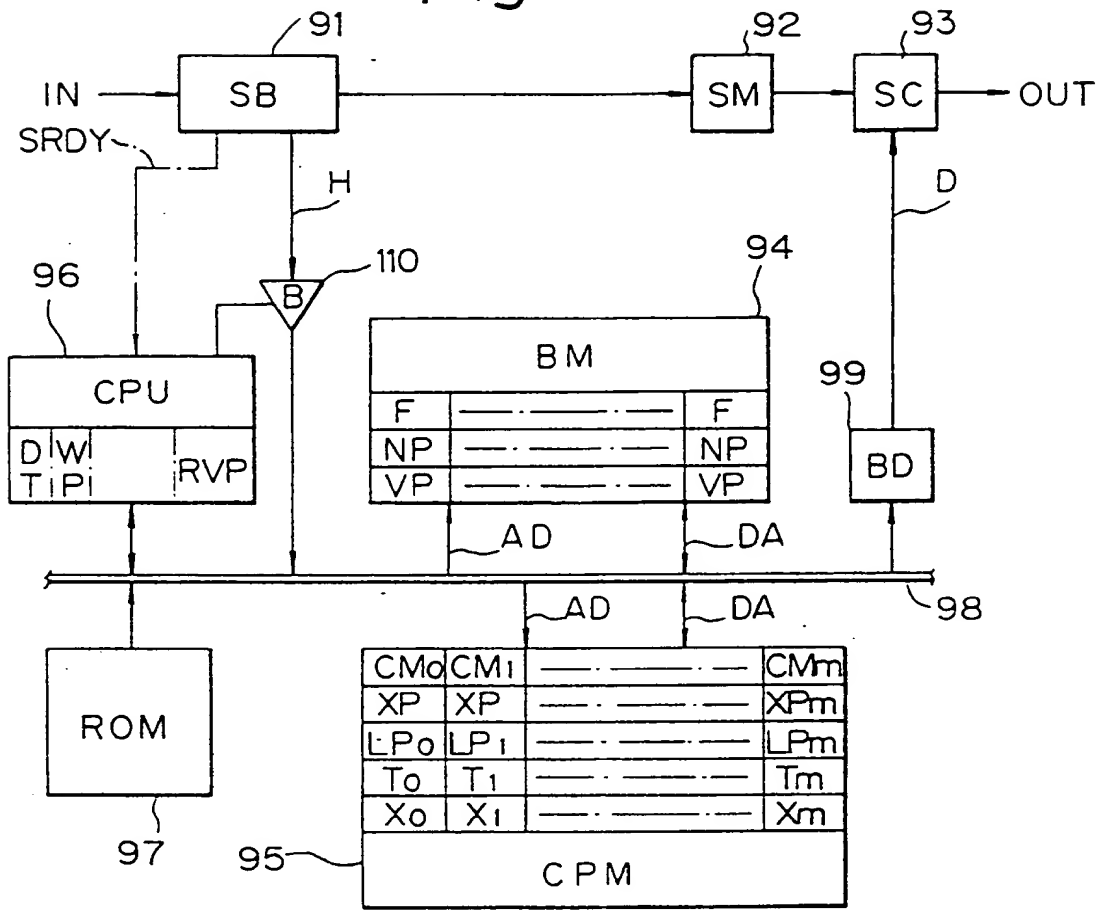

91
92
93
IN
SB
SM
SC
OUT
SRDY
H
D
110
94
96
B
BM
99
CPU
F
F
NP
NP
VP
VP
D W
T P
RVP
BD
AD
DA
98
AD
DA
CMo CM1
CMm
XP XP
XPm
LPo LP1
LPm
To T1
Tm
Xo X1
Xm
ROM
97
95
CPM

Fig. 9B

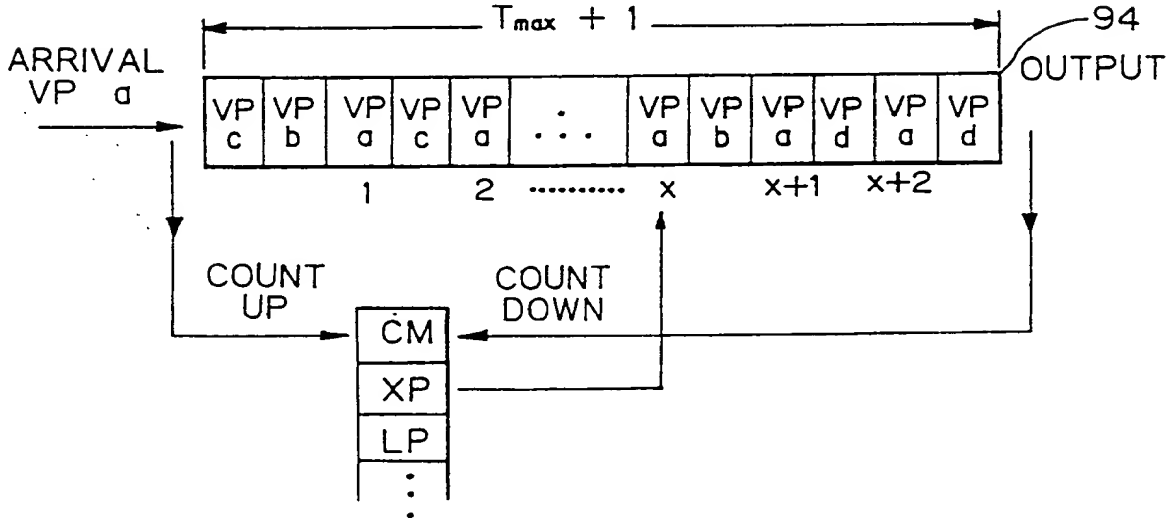

Tmax + 1
94
ARRIVAL
VP a
OUTPUT
VP c
VP b
VP a
VP c
VP a
VP a
VP b
VP a
VP d
VP a
VP d
1
2
x
x+1
x+2
COUNT
UP
COUNT
DOWN
CM
XP
LP

Fig. 10

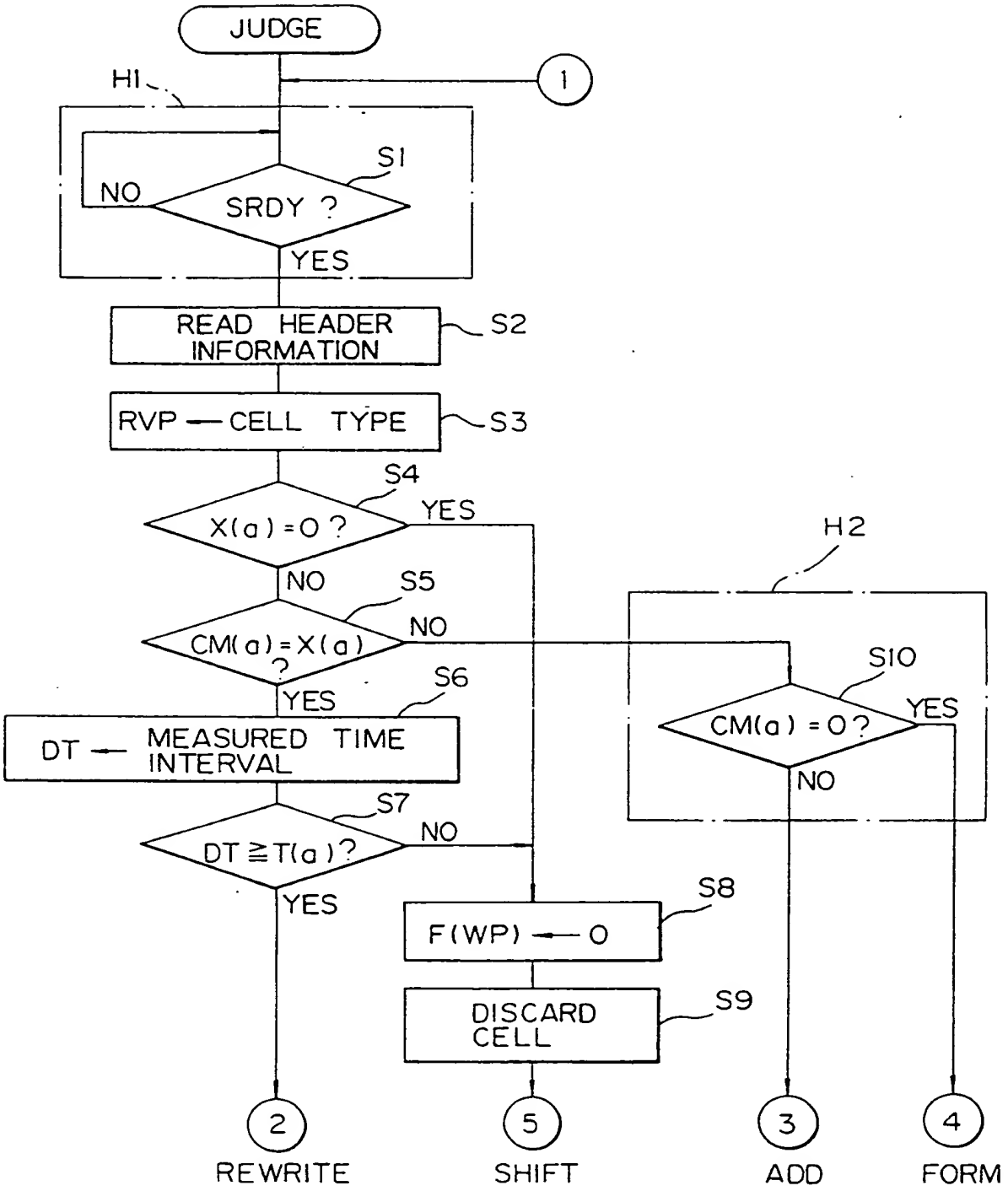

JUDGE
H1
1
S1
NO
SRDY ?
YES
READ HEADER INFORMATION
S2
RVP — CELL TYPE
S3
S4
X(a) = 0 ?
YES
NO
S5
CM(a) = X(a) ?
NO
YES
S6
DT — MEASURED TIME INTERVAL
S7
DT ≧ T(a) ?
NO
YES
H2
S10
CM(a) = 0 ?
YES
NO
S8
F(WP) — 0
DISCARD CELL
S9
2
REWRITE
5
SHIFT
3
ADD
4
FORM

Fig. 11

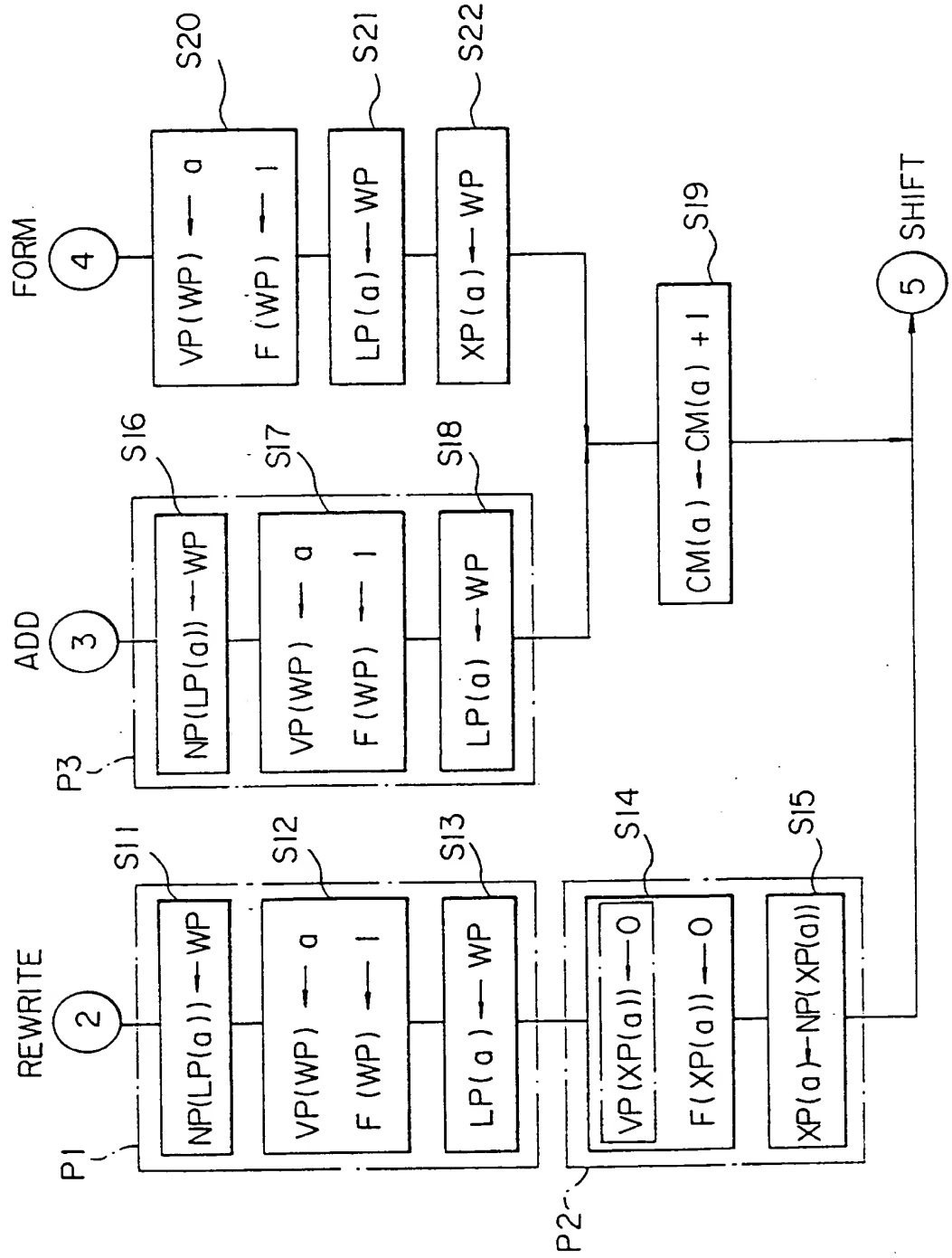

REWRITE
2
P1
S11
NP(LP(a)) — WP
S12
VP(WP) — a
F(WP) — 1
S13
LP(a) — WP
P2
S14
VP(XP(a)) — 0
F(XP(a)) — 0
S15
XP(a) — NP(XP(a))
ADD
3
P3
S16
NP(LP(a)) — WP
S17
VP(WP) — a
F(WP) — 1
S18
LP(a) — WP
FORM
4
S20
VP(WP) — a
F(WP) — 1
S21
LP(a) — WP
S22
XP(a) — WP
S19
CM(a) — CM(a) + 1
5
SHIFT

Fig. 12

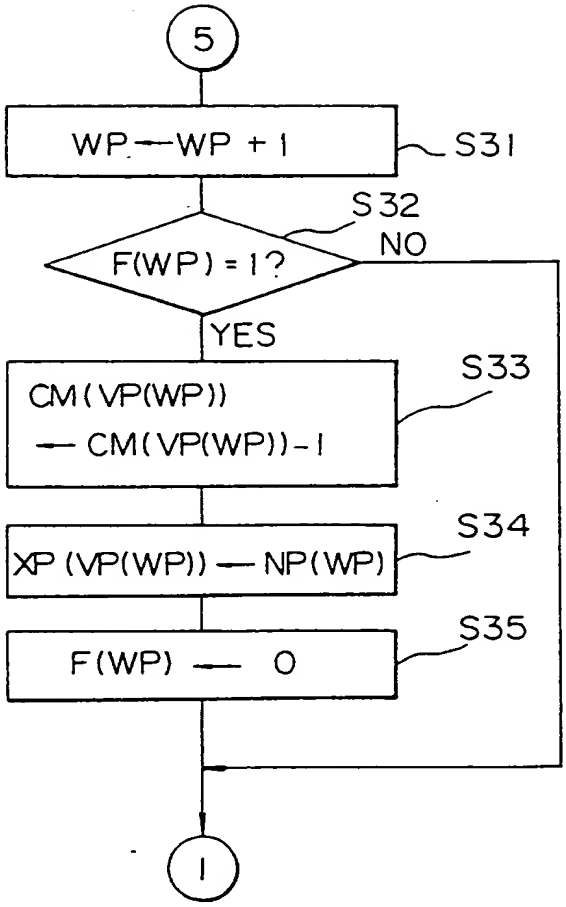

5
WP ← WP + 1
S31
S32
F(WP) = 1?
NO
YES
S33
CM(VP(WP))
← CM(VP(WP))-1
S34
XP(VP(WP)) ← NP(WP)
S35
F(WP) ← 0
1

Fig. 13A

(JUDGE)

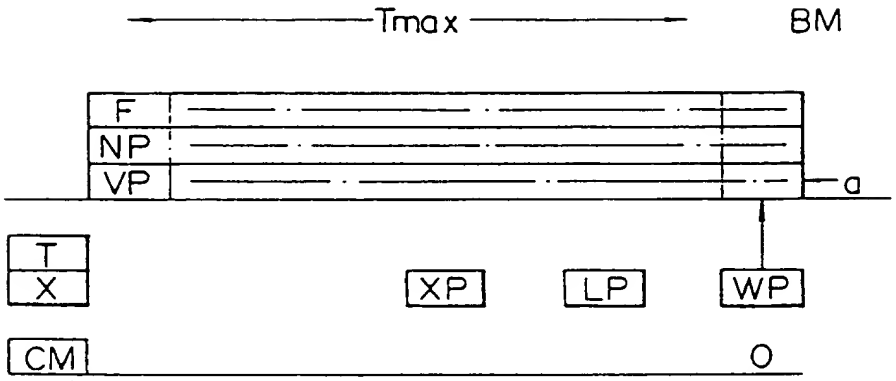


Fig. 13B

(FORM)

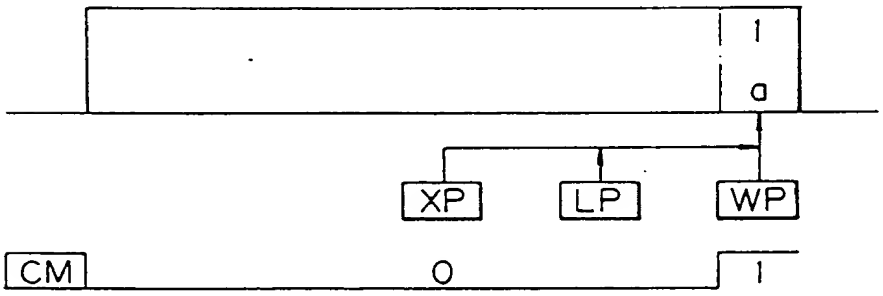


Fig. 13C

(SHIFT)

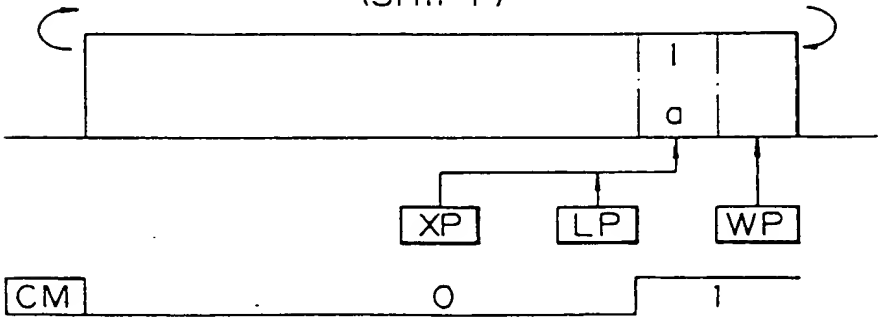


Fig. 14A

(JUDGE)

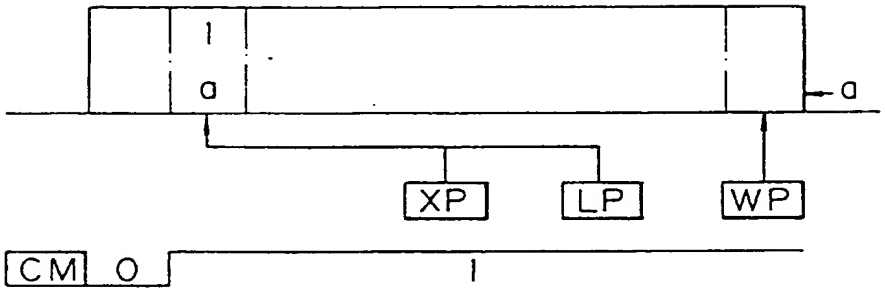


Fig. 14B

(ADD)

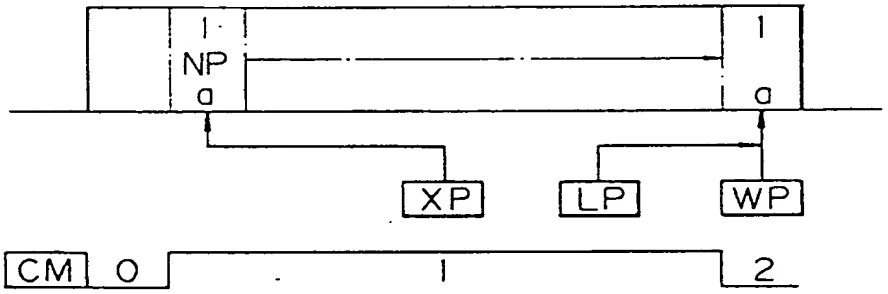


Fig. 14C

(SHIFT)

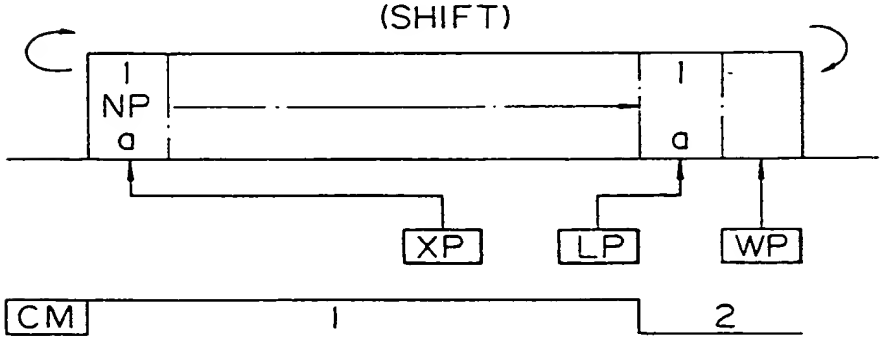


Fig. 15A

(JUDGE)

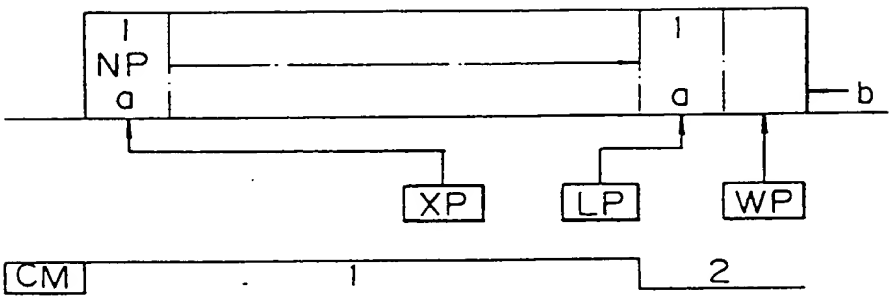


Fig. 15B

(FORM)

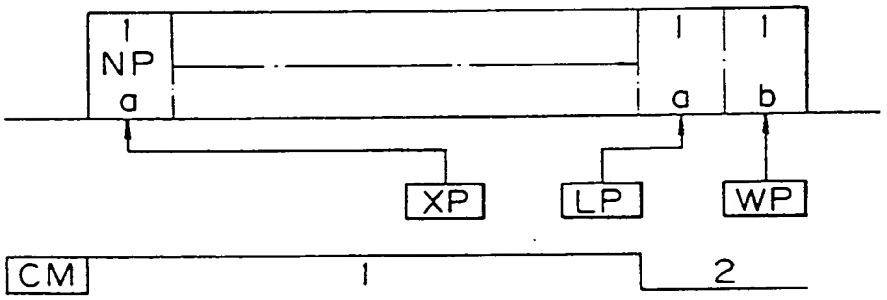


Fig. 15C

(SHIFT)

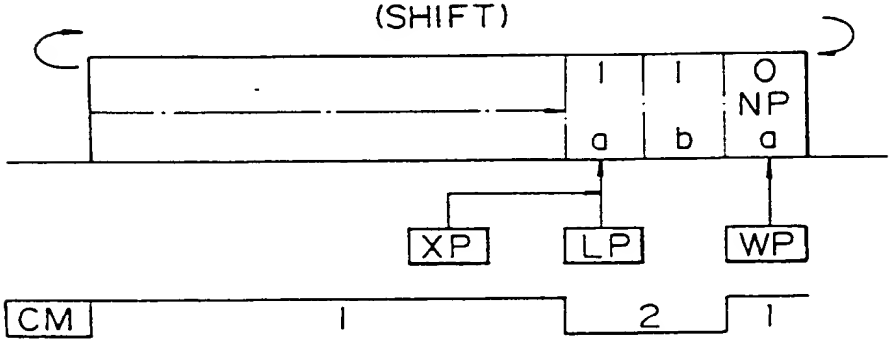


Fig. 16A

(JUDGE)

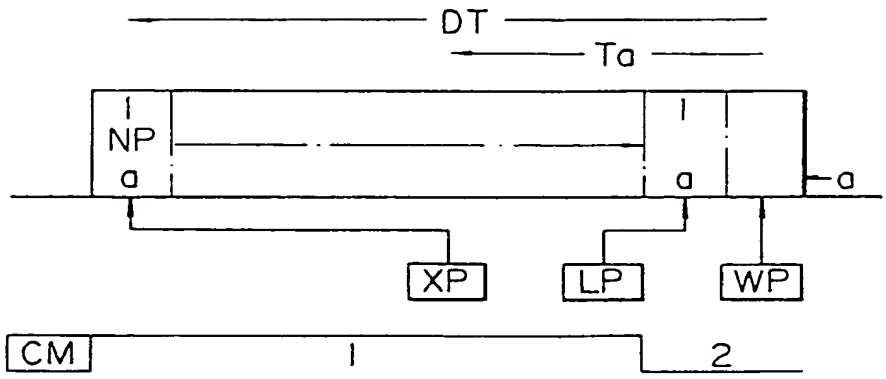


Fig. 16B

(REWRITE)

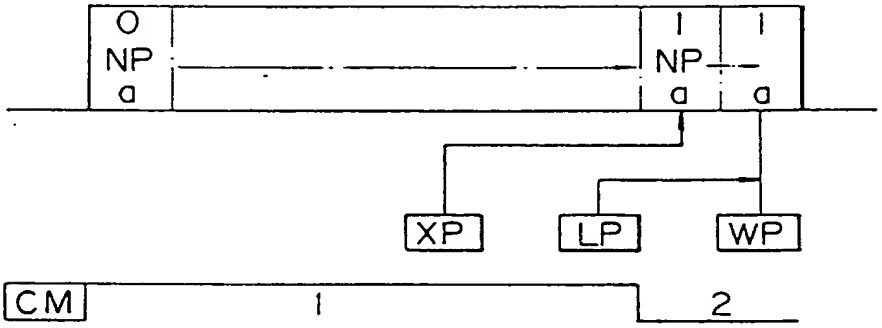


Fig. 16C

(SHIFT)

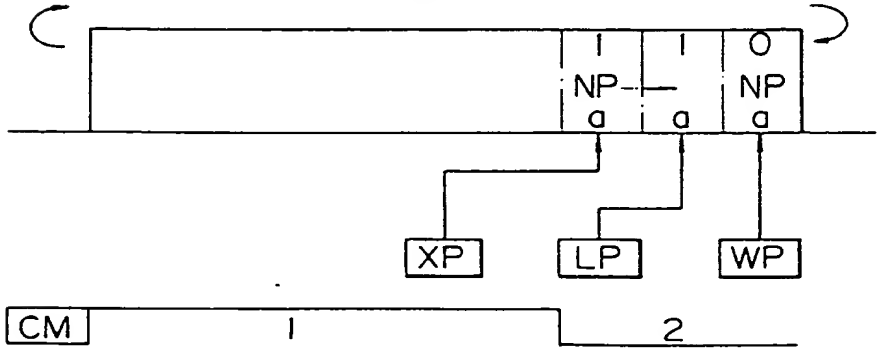


Fig. 17A

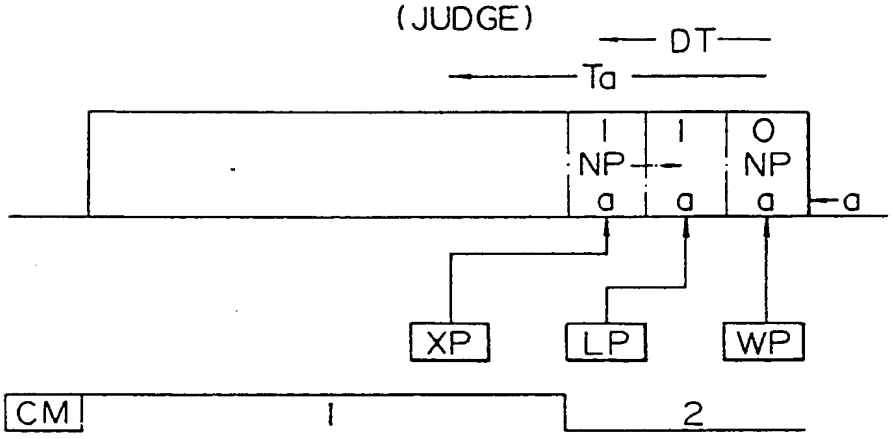


Fig. 17B

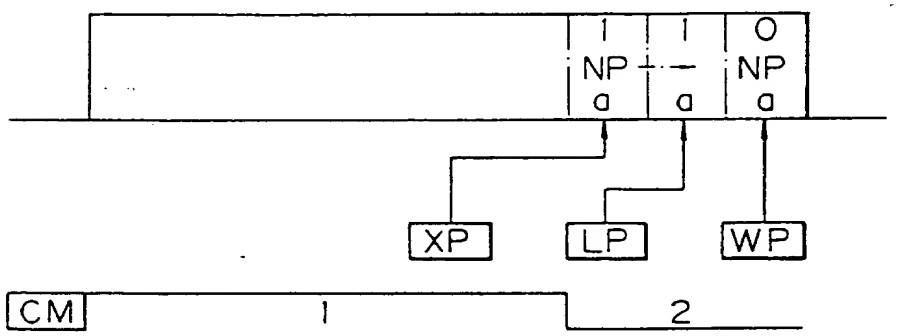


Fig. 17C

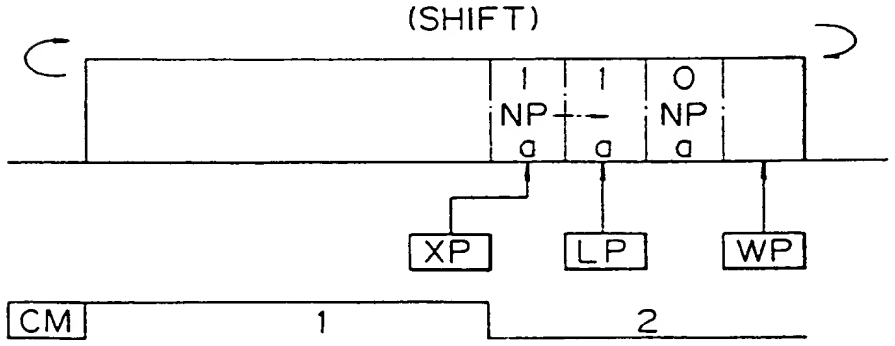


Fig. 18A

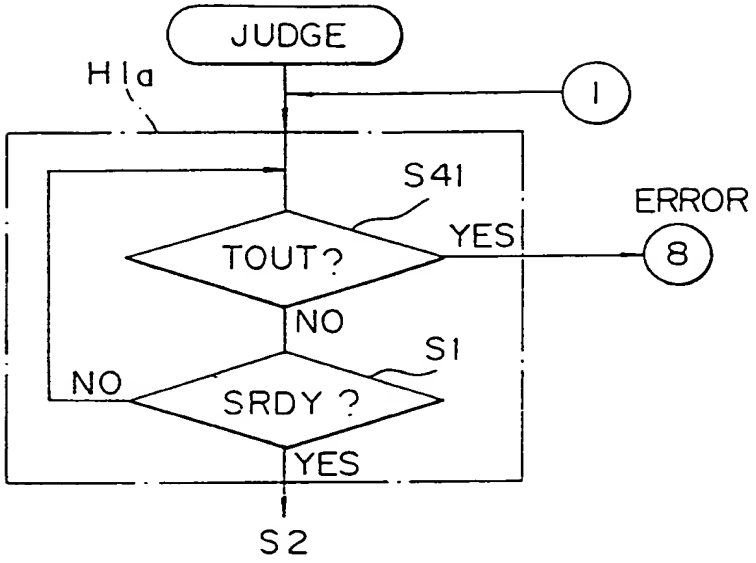


Fig. 18B

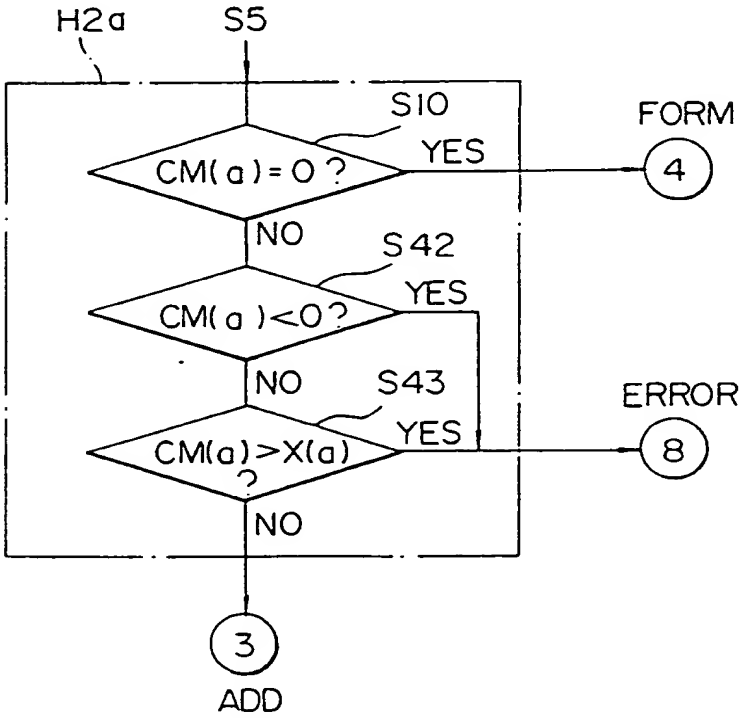


Fig. 19A

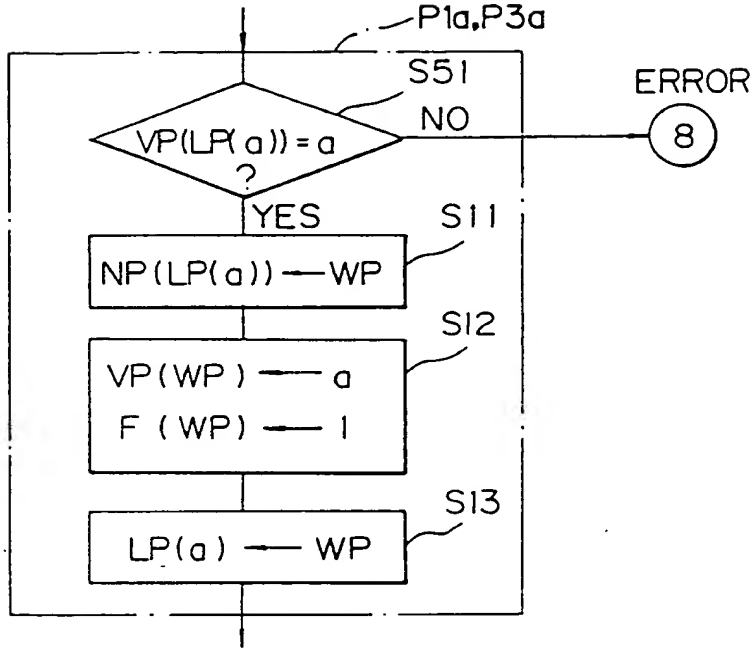


Fig. 19B

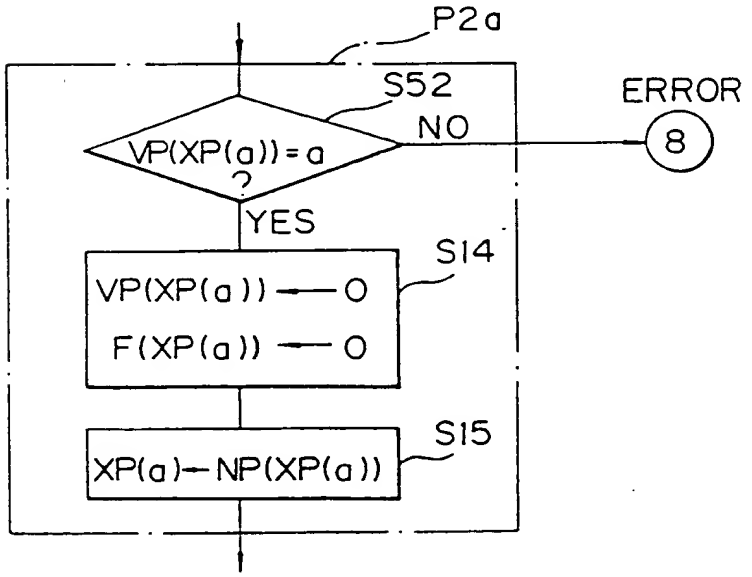


Fig. 20

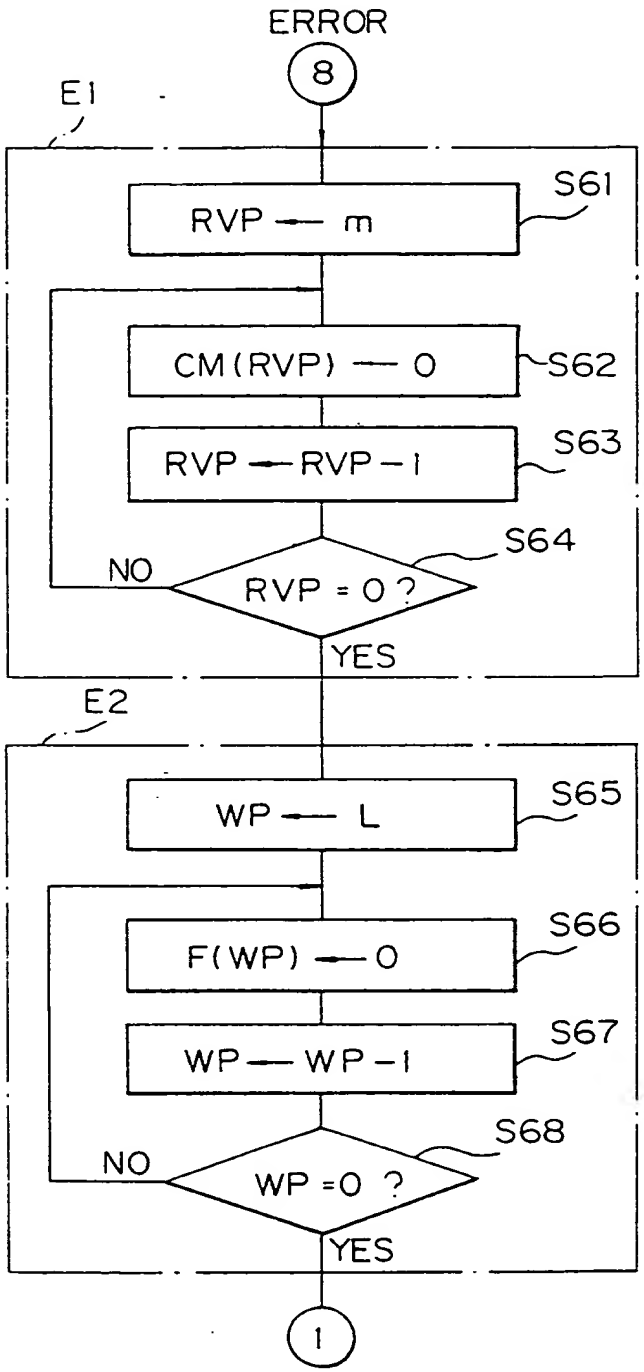

ERROR
8
E1
S61
RVP — m
CM(RVP) — 0
S62
RVP — RVP - 1
S63
S64
NO
RVP = 0 ?
YES
E2
S65
WP — L
S66
F(WP) — 0
S67
WP — WP - 1
S68
NO
WP = 0 ?
YES
1

Fig. 21

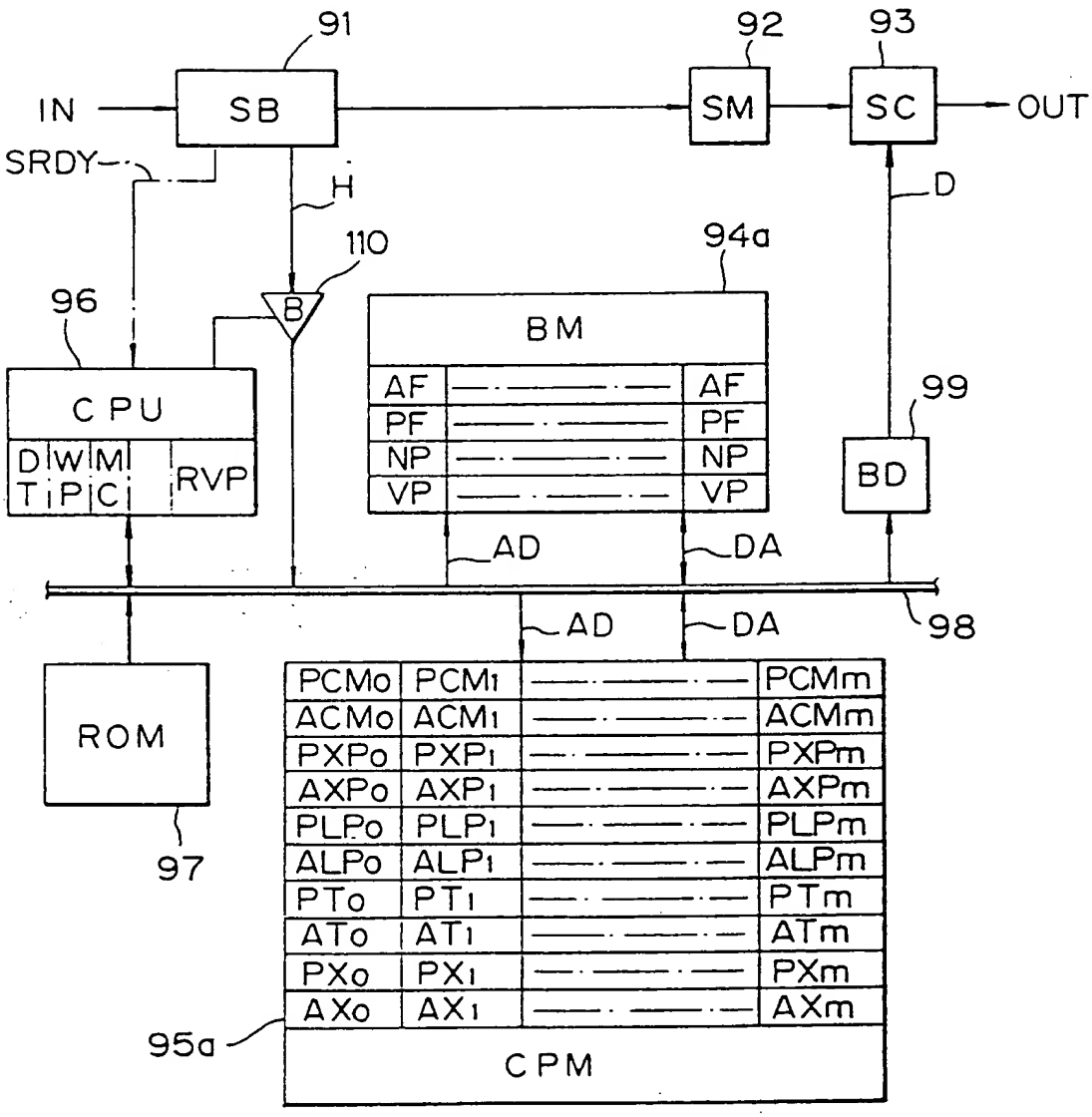

91
92
93
IN
SB
SM
SC
OUT
SRDY
H
D
110
94a
96
B
BM
AF
PF
NP
VP
CPU
DWTMPIC
RVP
99
BD
AD
DA
98
ROM
97
PCMo PCM1 PCMm
ACMo ACM1 ACMm
PXPo PXP1 PXPm
AXPo AXP1 AXPm
PLPo PLP1 PLPm
ALPo ALP1 ALPm
PTo PT1 PTm
ATo AT1 ATm
PXo PX1 PXm
AXo AX1 AXm
95a
CPM

Fig. 22

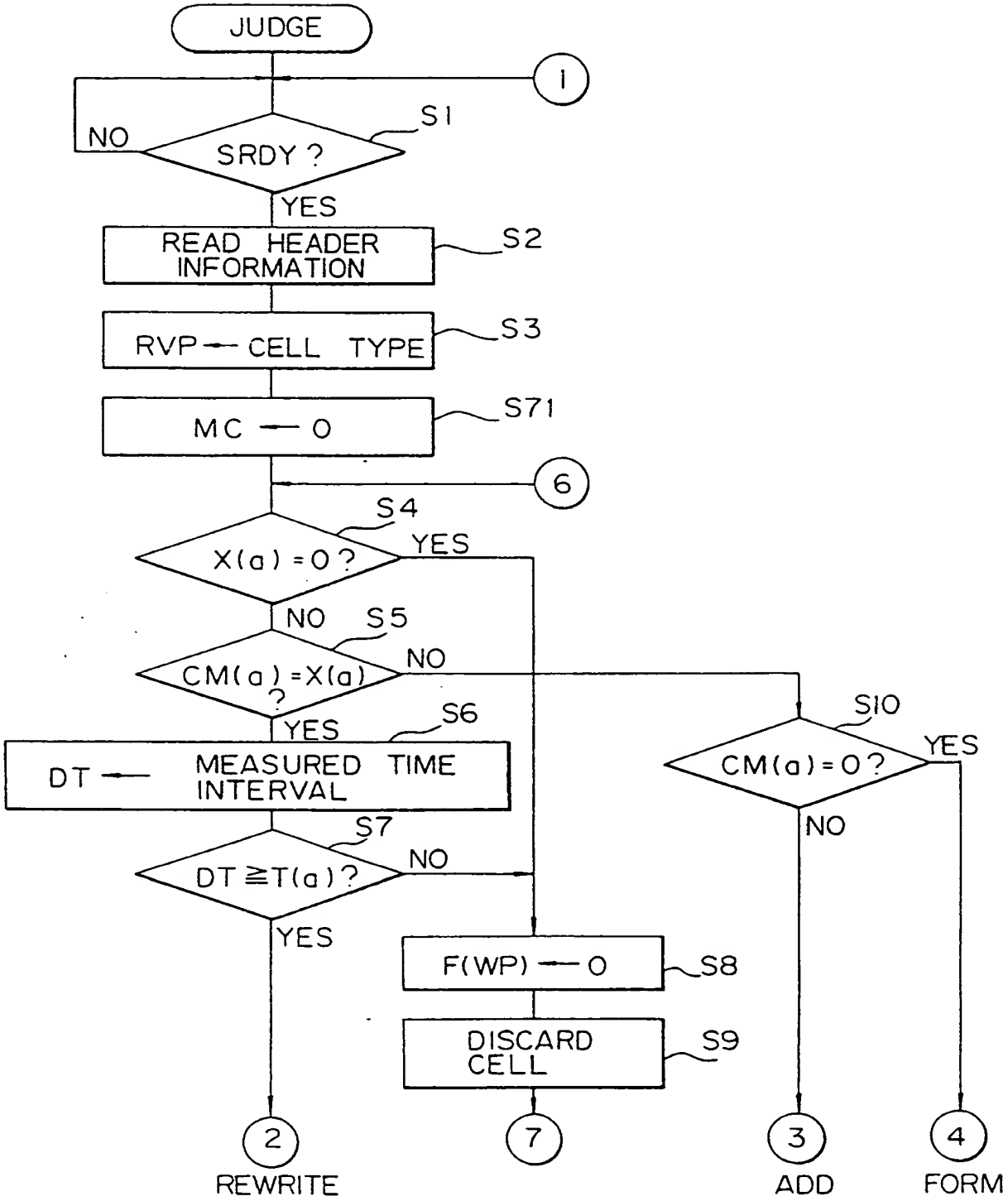

JUDGE
1
S1
NO
SRDY ?
YES
READ HEADER INFORMATION
S2
RVP ← CELL TYPE
S3
MC ← 0
S71
6
S4
X(a) = 0 ?
YES
NO
S5
CM(a) = X(a) ?
NO
YES
S6
DT ← MEASURED TIME INTERVAL
S7
DT ≧ T(a) ?
NO
YES
S10
CM(a) = 0 ?
YES
NO
F(WP) ← 0
S8
DISCARD CELL
S9
2
REWRITE
7
3
ADD
4
FORM

Fig. 23

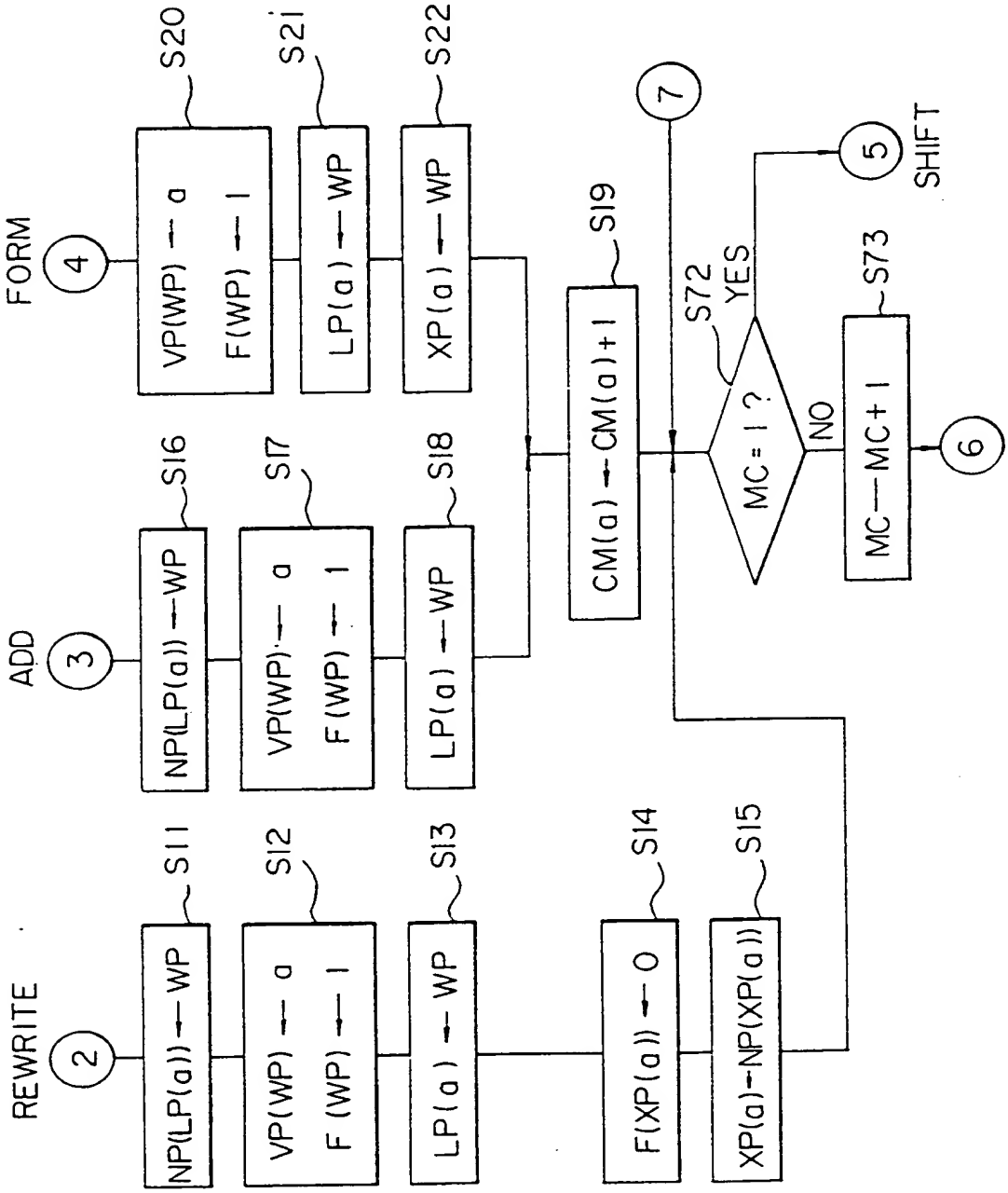

REWRITE
2
NP(LP(a)) ← WP
S11
VP(WP) ← a
F(WP) ← 1
S12
LP(a) ← WP
S13
ADD
3
NP(LP(a)) ← WP
S16
VP(WP) ← a
F(WP) ← 1
S17
LP(a) ← WP
S18
FORM
4
VP(WP) ← a
F(WP) ← 1
S20
LP(a) ← WP
S21
XP(a) ← WP
S22
F(XP(a)) ← 0
S14
XP(a) ← NP(XP(a))
S15
CM(a) ← CM(a) + 1
S19
7
S72
MC = 1 ?
YES
NO
5
SHIFT
MC ← MC + 1
S73
6

Fig. 24

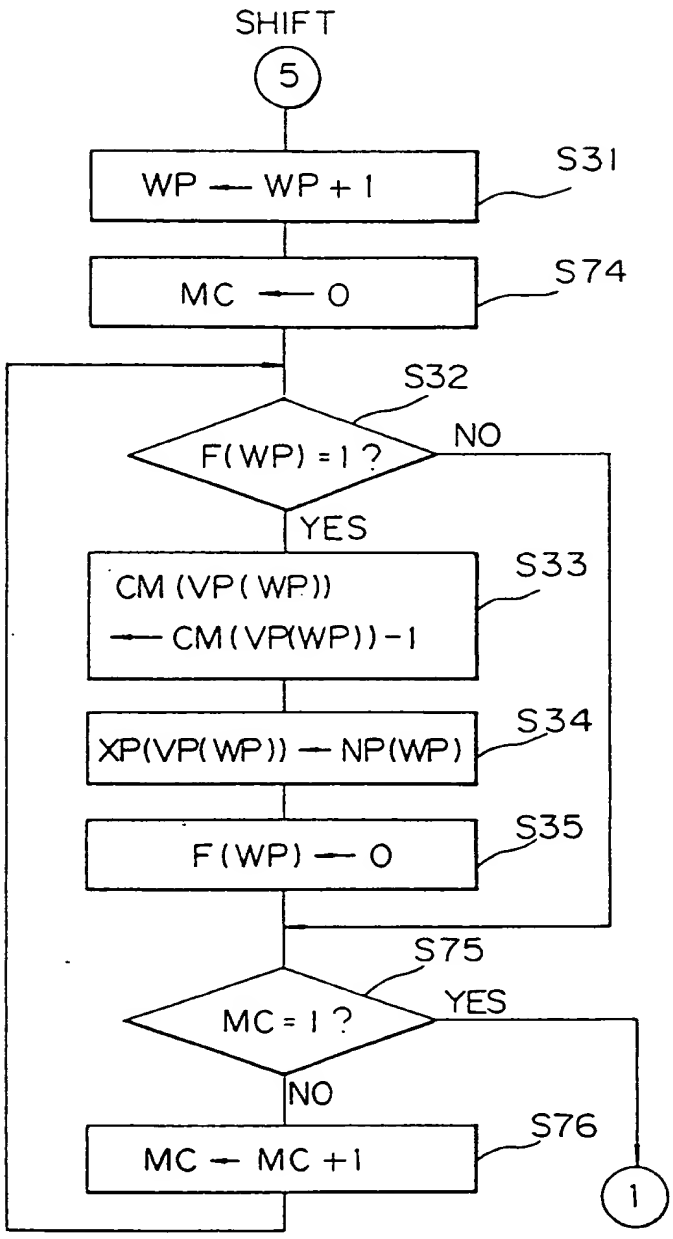

SHIFT
5
WP — WP + 1
S31
MC — 0
S74
S32
F(WP) = 1 ?
NO
YES
CM (VP(WP))
— CM(VP(WP)) - 1
S33
XP(VP(WP)) — NP(WP)
S34
F(WP) — 0
S35
S75
MC = 1 ?
YES
NO
MC — MC + 1
S76
1

Fig. 25A

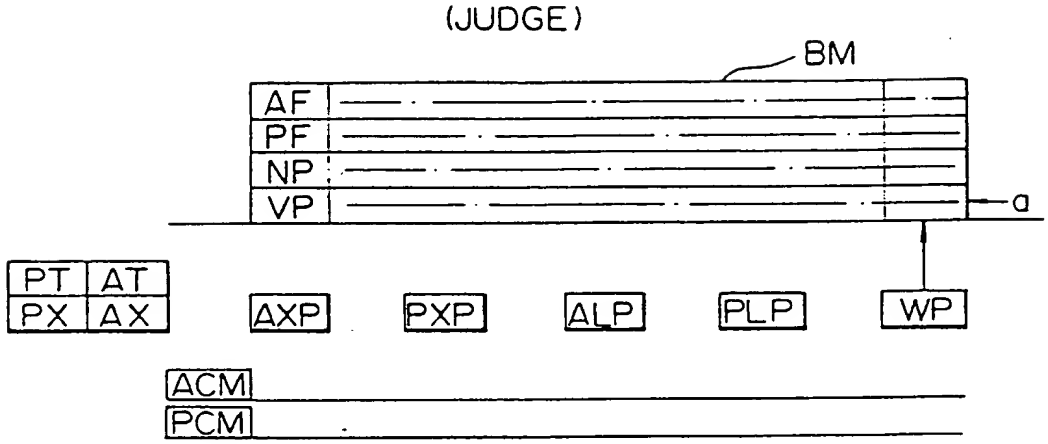


Fig. 25B

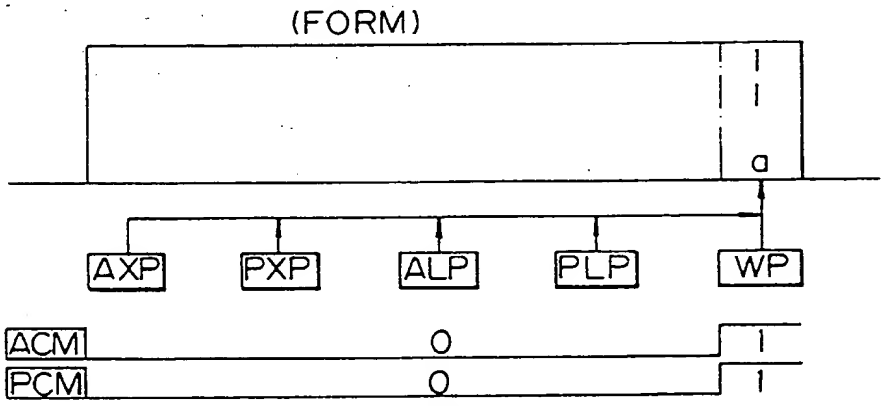


Fig. 25C

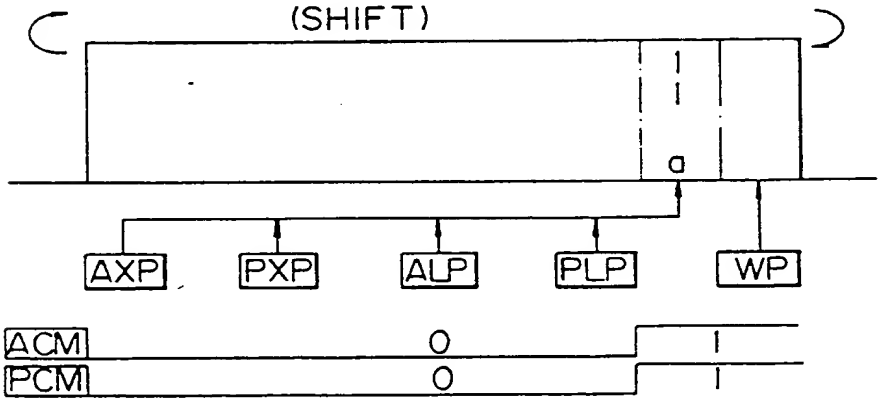


Fig. 26A

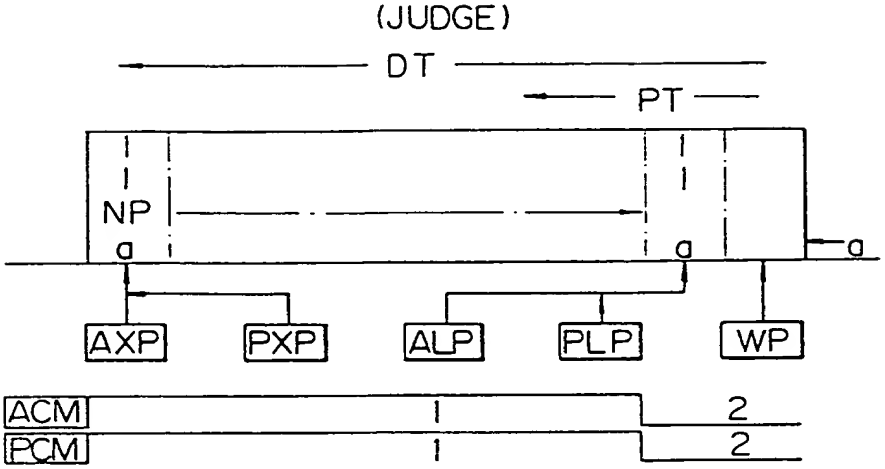


Fig. 26B

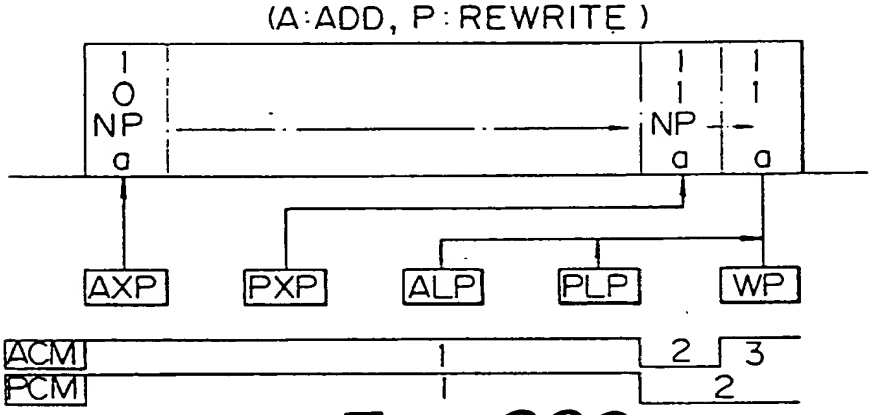


Fig. 26C

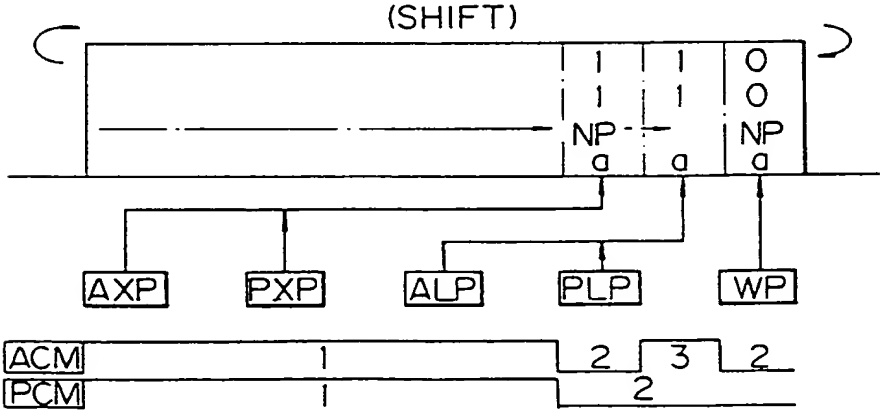


Fig. 27A (JUDGE)

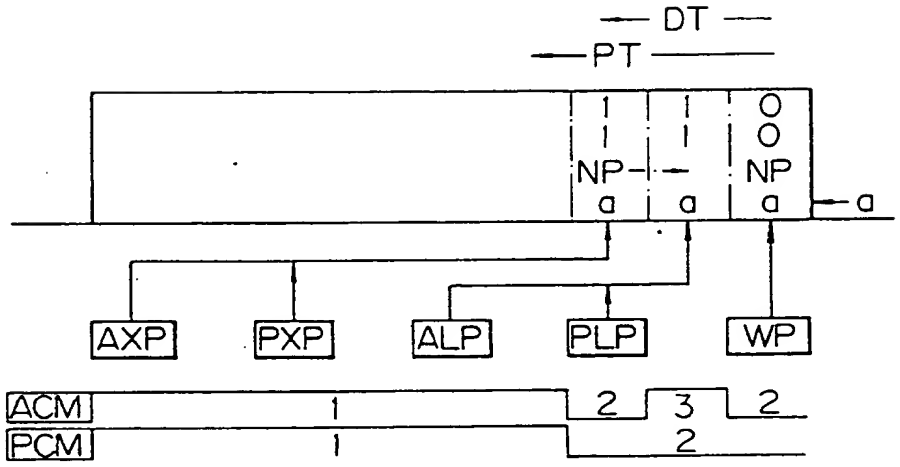


Fig. 27B (A:ADD, P:DISCARD)

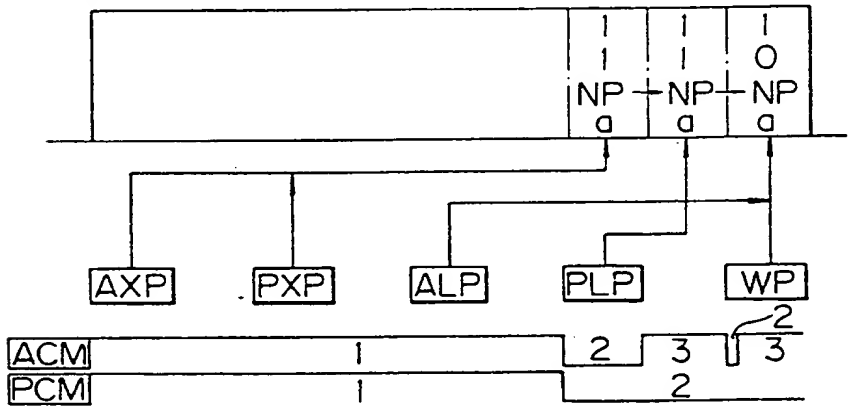


Fig. 27C (SHIFT)

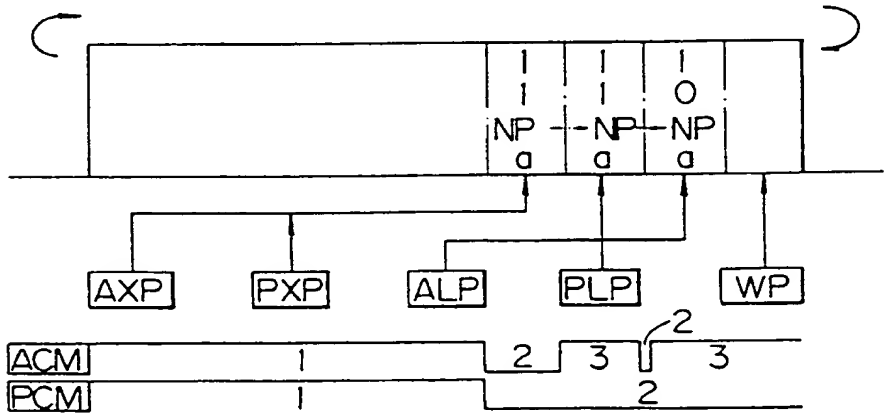


Fig. 28A PRIOR ART

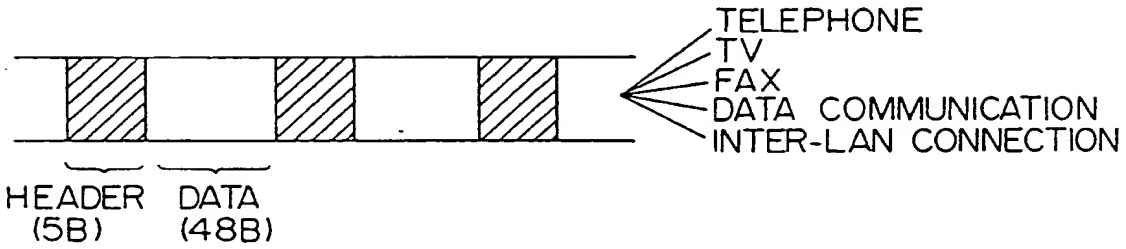


Fig. 28B PRIOR ART

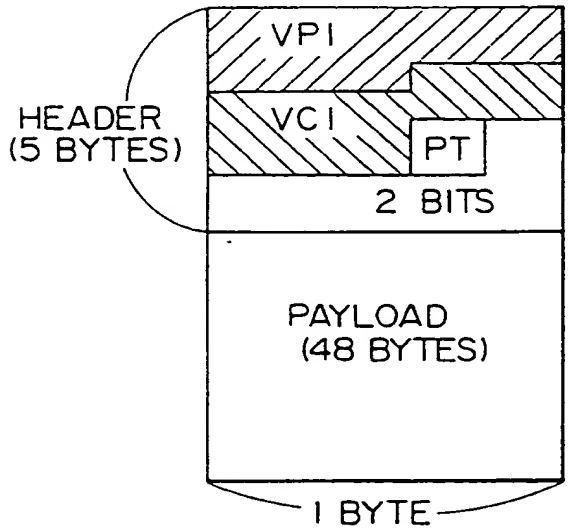


Fig. 29

TIME INTERVAL METHOD

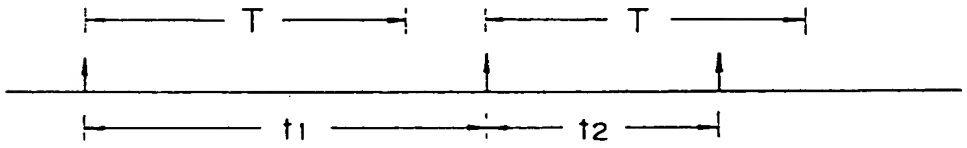


Fig. 30

T – X METHOD

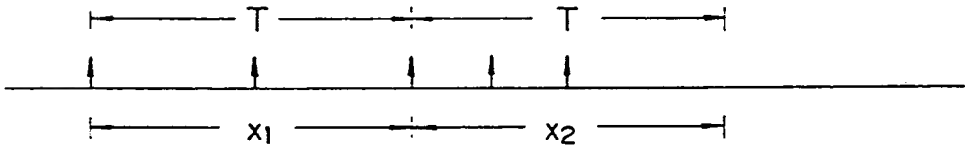


Fig. 31

DB METHOD

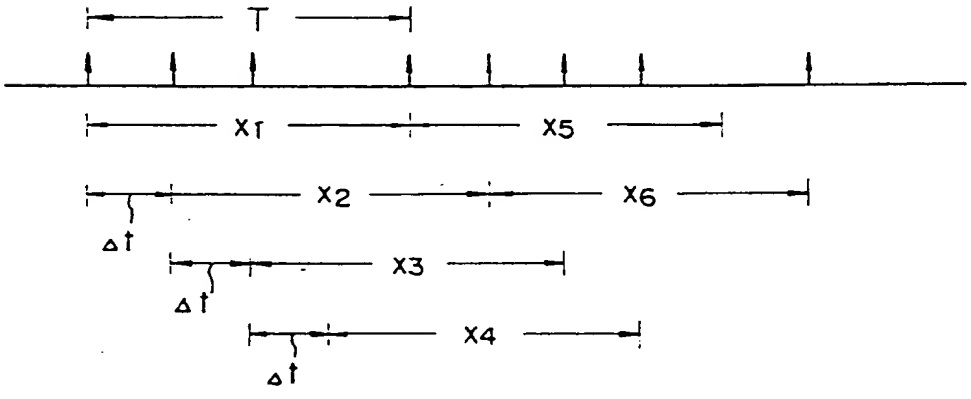
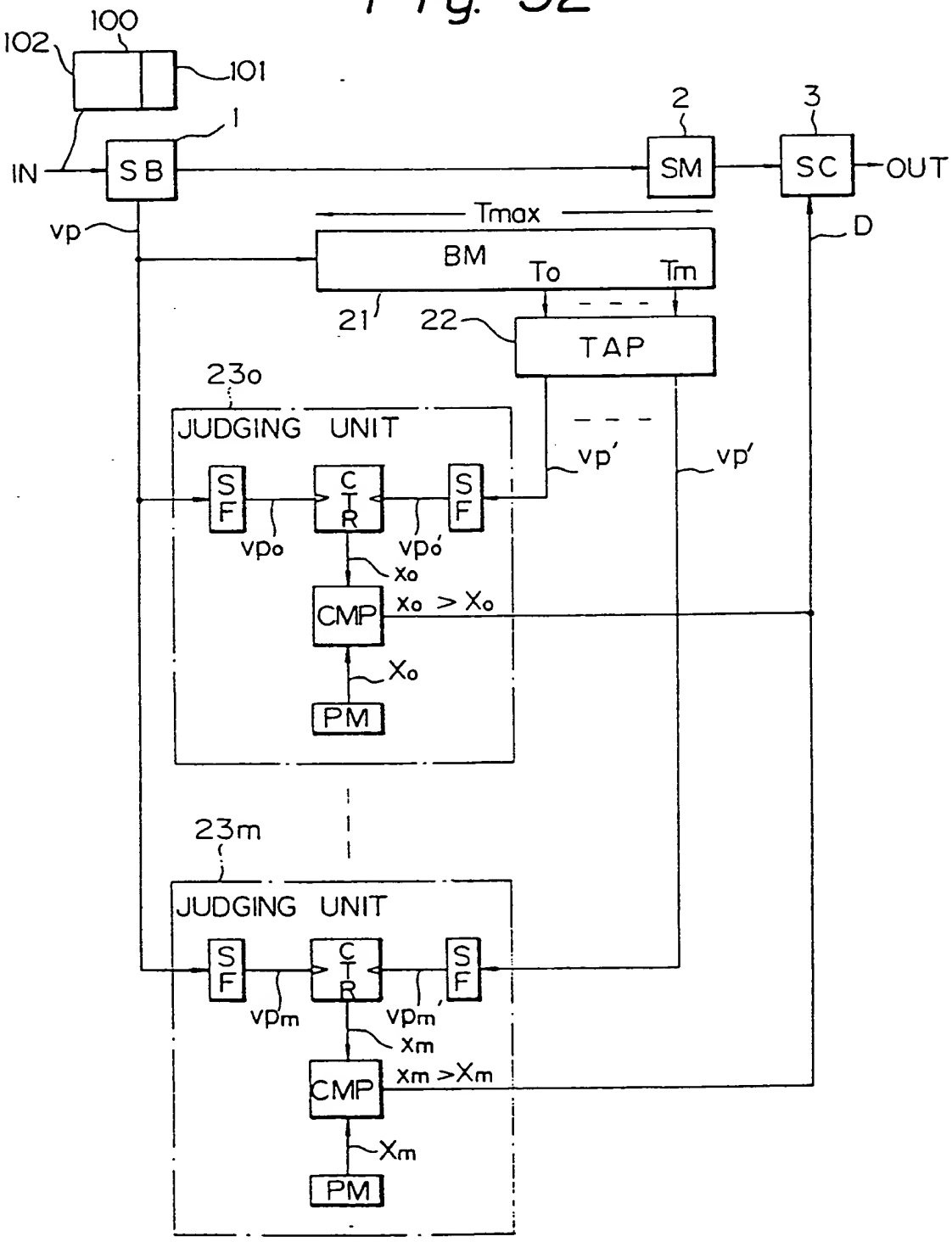


Fig. 32


100
102
101
1
IN
SB
2
SM
3
SC
OUT
vp
Tmax
D
BM
To
Tm
21
22
TAP
23o
JUDGING UNIT
SF
CTR
SF
vp'
vp'
vpo
vpo'
xo
CMP
xo > Xo
Xo
PM
23m
JUDGING UNIT
SF
CTR
SF
vpm
vpm'
xm
CMP
xm >Xm
Xm
PM